



H61H2-M17

Rev : 1.0

ECS CONFIDENTIAL

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24	AUDIO VT1705/ALC662(CHIP)
25	AUDIO VT1705/ALC662(PANEL)


NOTE:

Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_2_1.pdf,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip

REVISION HISTORY:

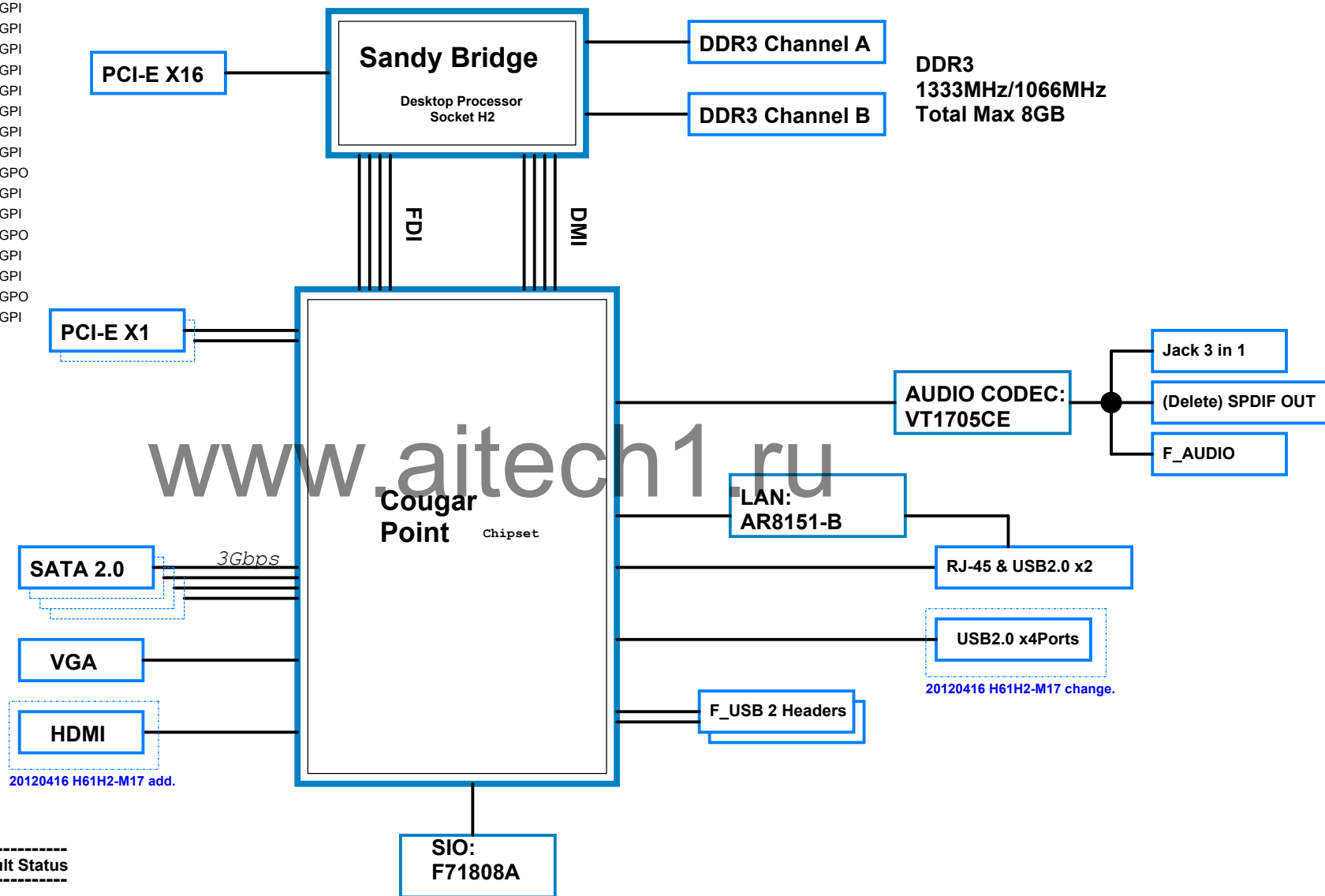
Rev	Date	Notes
P61G V1.0	2011/04/07	RED_PCB P/N : 15-Y97-011001 (GE1) / 15-Y97-011000 (CHUANYI) BOM P/N : 81-605-Y97100 EC35 change to EC-cap 1000U-6.3DL EC1, EC4 from 100uF change to 220uF Del RT1, RT3, R137, R180 (Not need compensation of temperature). For 5VSB Inrush Current : R102 from 100k change to 33k. Select TACH0_GPIO17 to decide COM .
H61H2-M12 VA	2011/05/04	Black_PCB P/N : 15-EC7-010010 BOM P/N : 81-605-EC7000/81-605-EC7001(10/100 ; GIGA) PCB Size change to 225*170 mm Del DVI Vcore 減少一相 VIN 電容減少一顆 LAN change to Atheros 8152/8151/8161 Codec change to VT1705CE. USB Power use fuse & Jumper.
H61H2-M12 V1.0	2011/07/12	Black_PCB P/N : 15-EC7-011000/15-EC7-011001 BOM P/N : 89-206-EC7100 / 89-206-EC7101 (10_100 / GIGA) Page 17, Power VCC_DDC change to VCC. PCB Size change to 225*170 mm
H61H2-M17 V1.0	2012/04/16	PAGE 9,10,11:Change CPU VRM solution to Richtek. PAGE 14&22:Add USB*2. PAGE 17&21:Add HDMI. PAGE 26:Change to Giga LAN AR8151-B default.

RD : Leon Tang
LAYOUT : Run Ouyang
EMI : Light Wang

 Elitegroup Computer Systems	
Title: Cover Page	
Size: Custom	Document Number: H61H2-M17
Date: Wednesday, May 02, 2012	Rev: 1.0
Sheet 1 of 29	

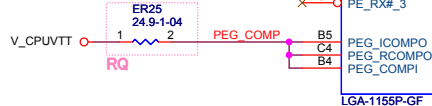
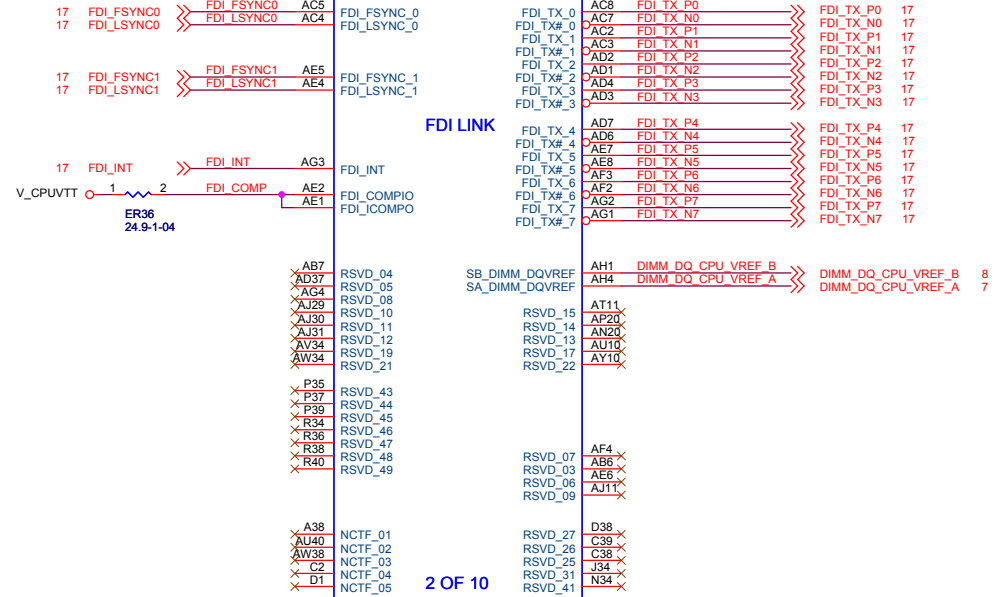
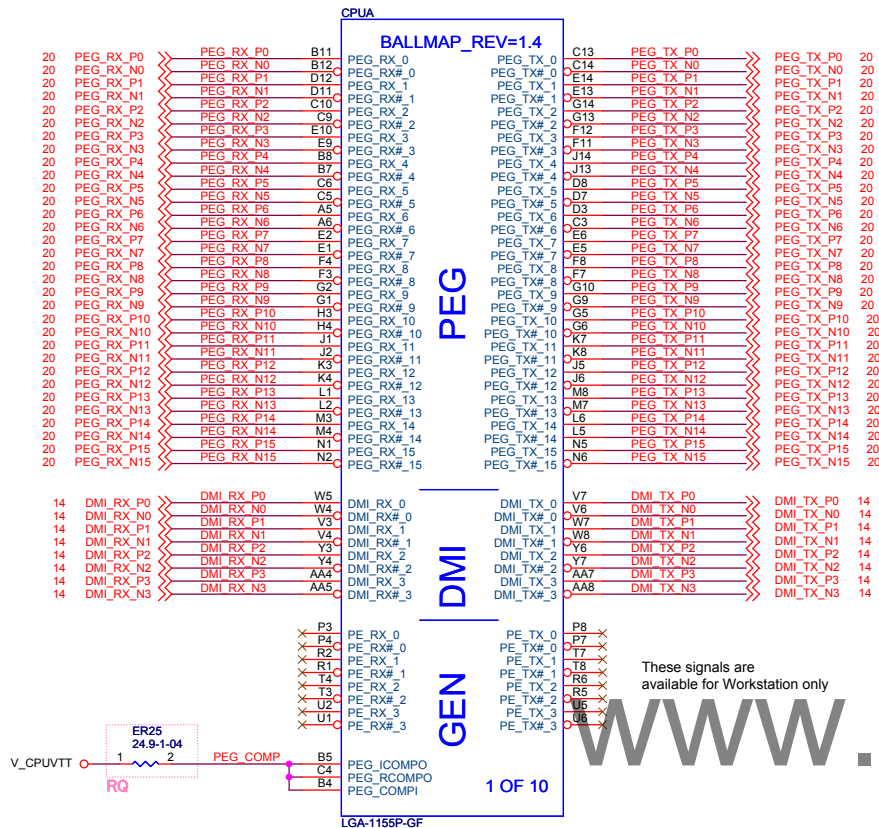
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI
GPIO15	3VSB	Down Voltage for DIMM	GPO
GPIO48	VCC3	Down Voltage for DIMM	GPI



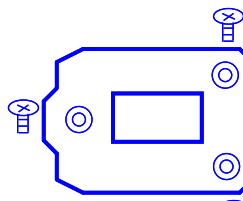
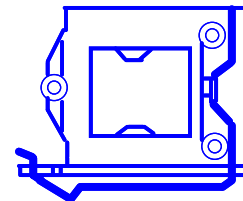
SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
PIN23	5VSB	Power LED	GPIO25/LEDVCC/WDTRST#
PIN22	5VSB	Power LED	GPIO24/LEDVSB
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

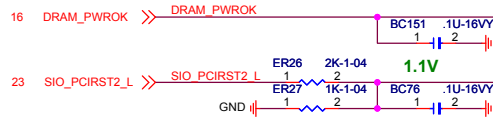
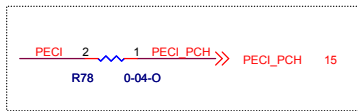


SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPARATE 12MIL TRACE.

CPU(104)
CPU_SUBASSY_STEEL



01D201-000060 PCH E50



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

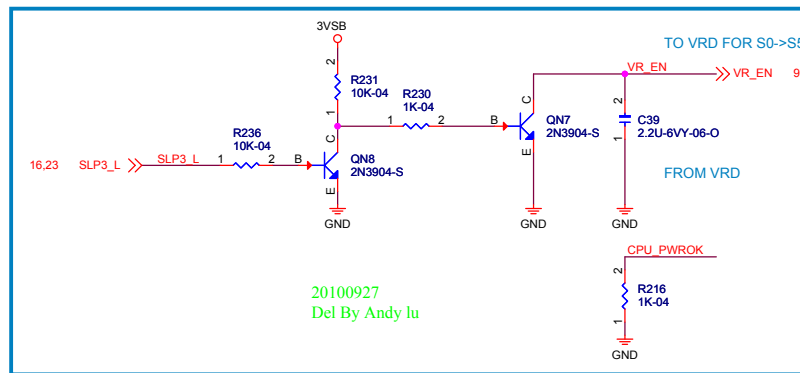
CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X2

change test point for internal PU Jack05/25

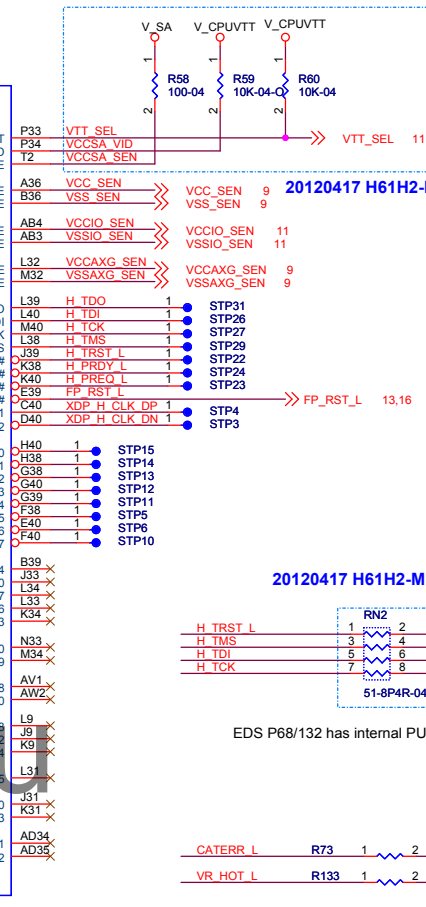
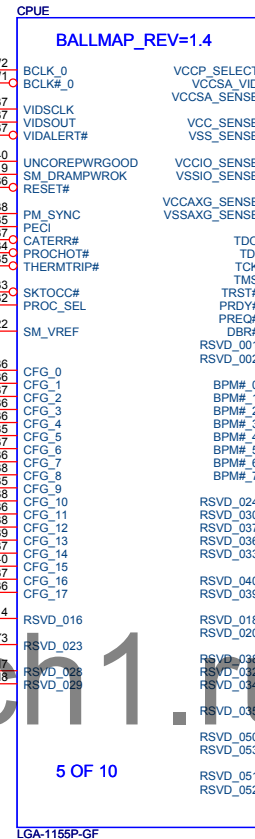
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5 OF 10

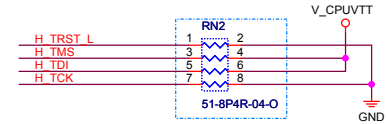
Power Down Sequencing Circuit



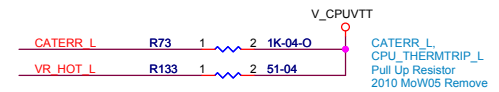
20100927
Del By Andy lu



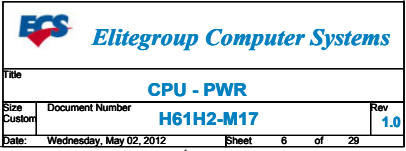
20120417 H61H2-M17 change.

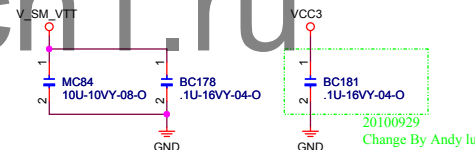
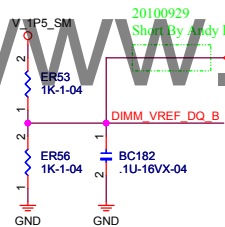
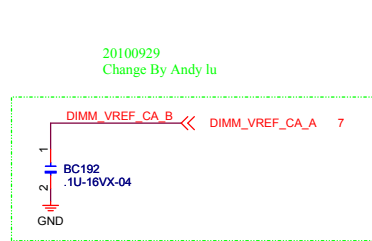
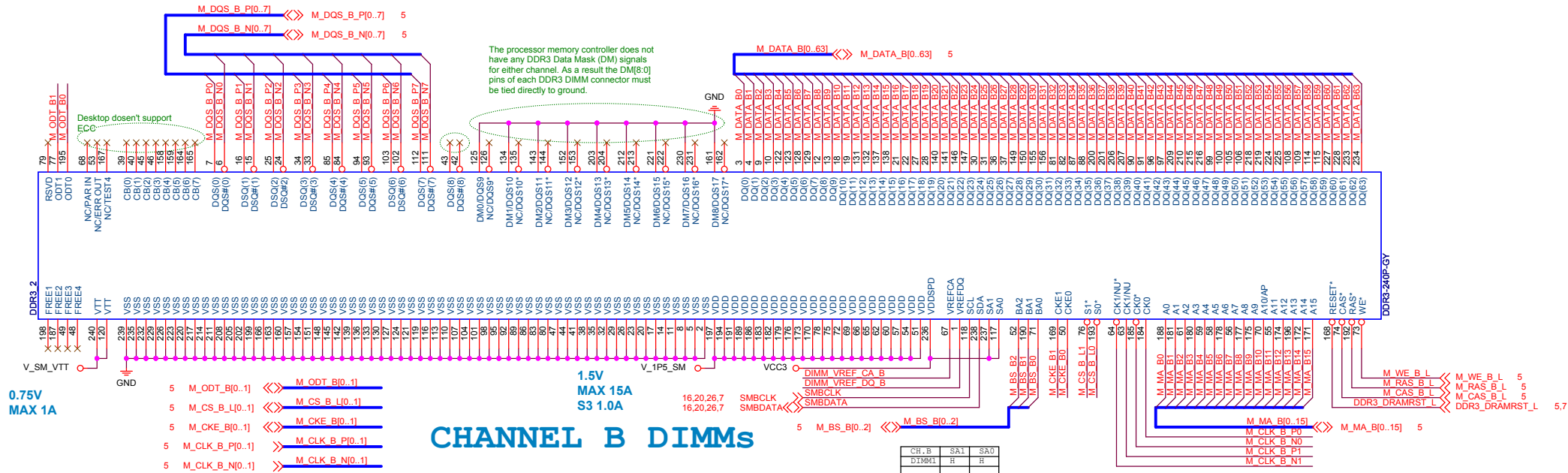


EDS P68/132 has internal PU Jack05/25



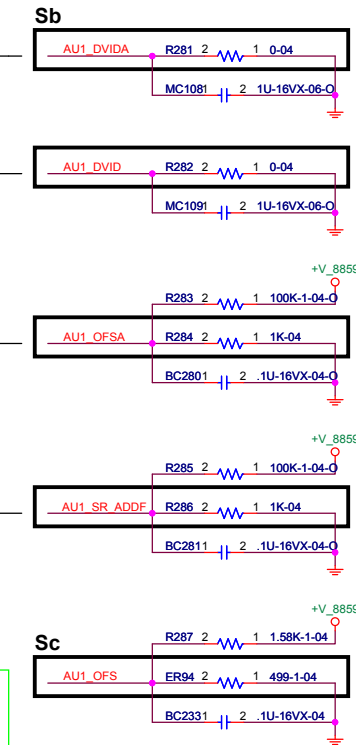
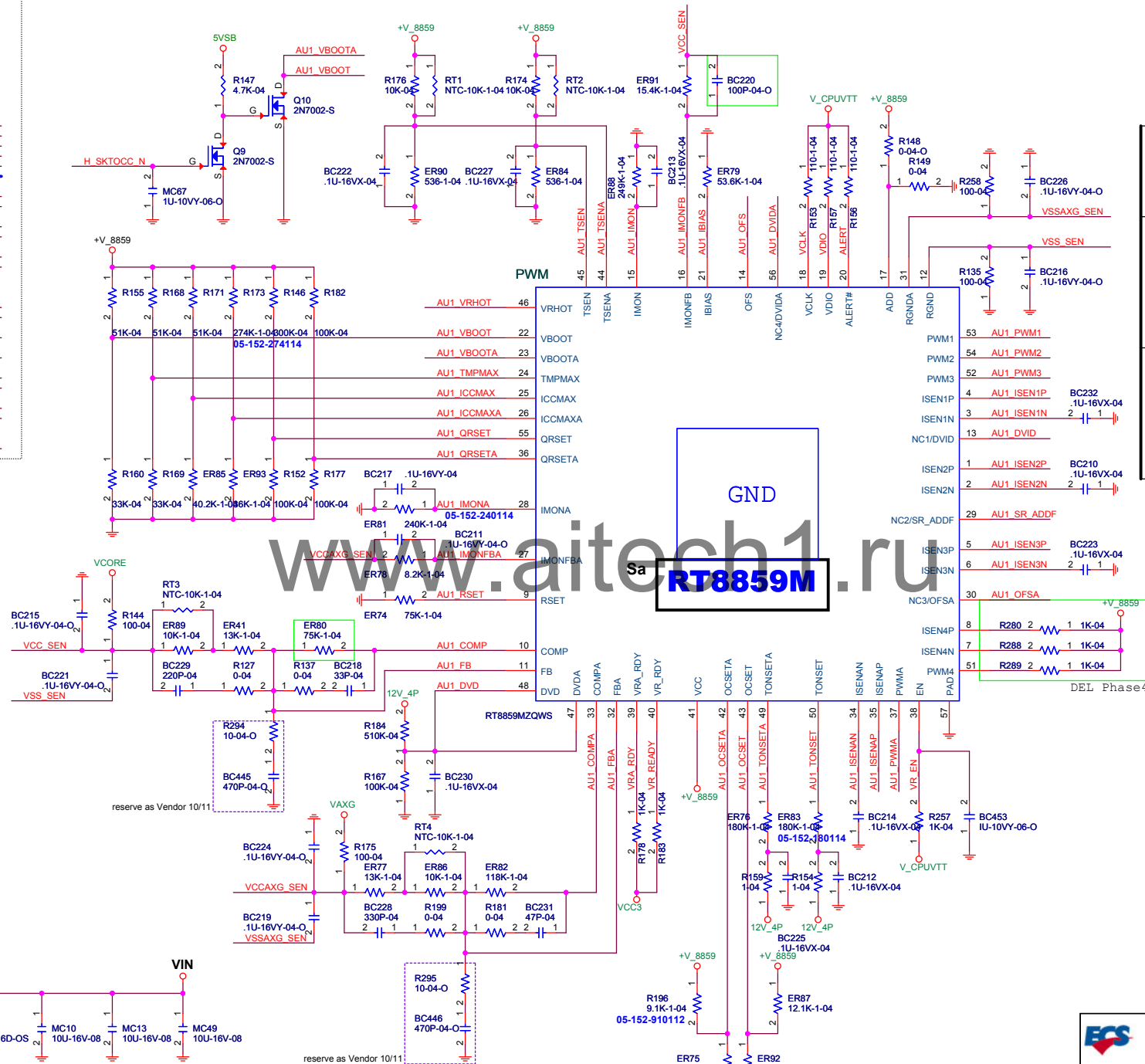
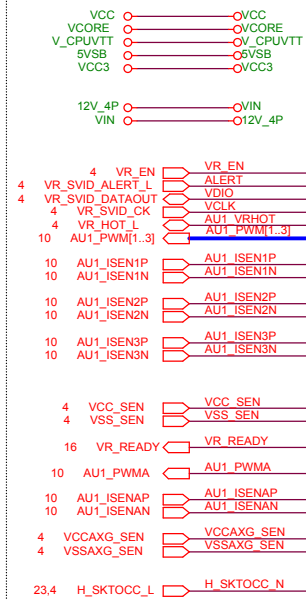
DMI/FDI termination voltage:
DC coupled: TX/RX to VCC ISF sampled high
DC coupled: TX/RX TO VSS IF sampled low
AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap





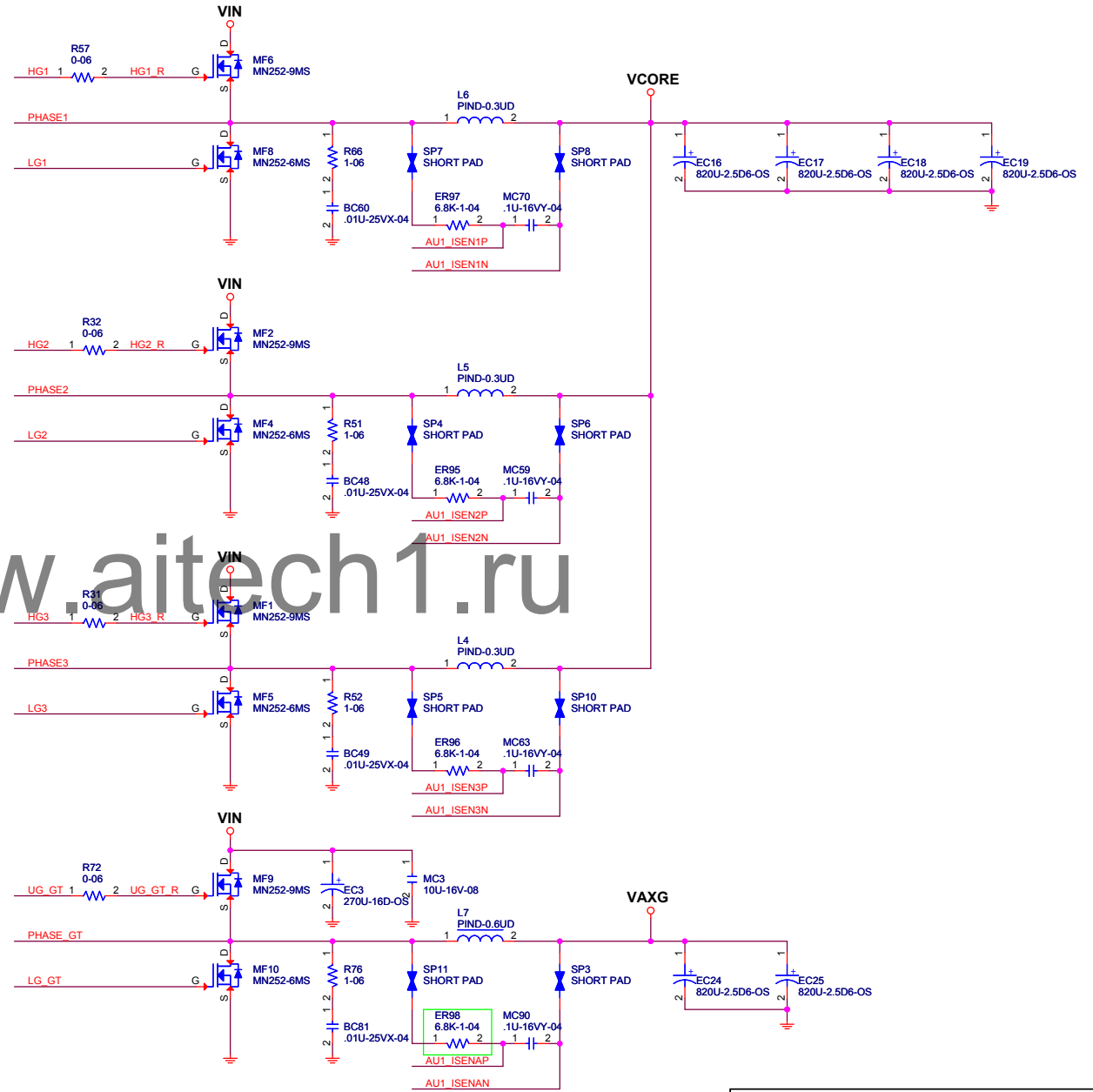
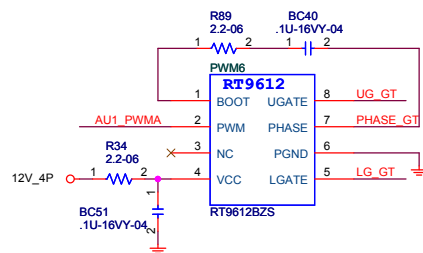
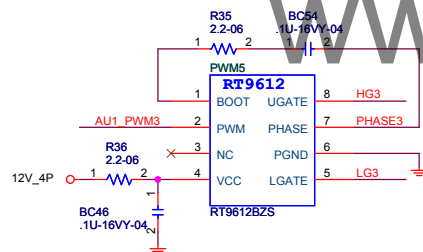
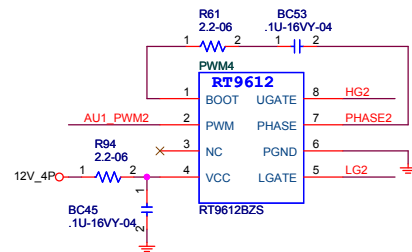
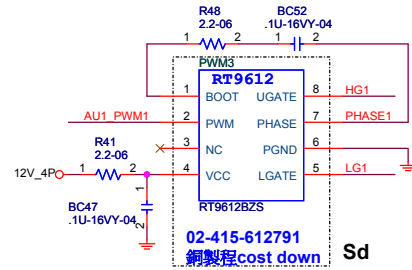
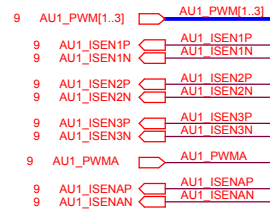
Del DIMM3 for always populate DIMM4 first Jack 05/13

External Connection



	RT8859A	RT8859M
Sa	RT8859A	RT8859M
Sb	X	V
Sc	402-1-04	499-1-04
	change 1K for OV	
Sd	RT9619	RT9612

External Connection



Elitegroup Computer Systems

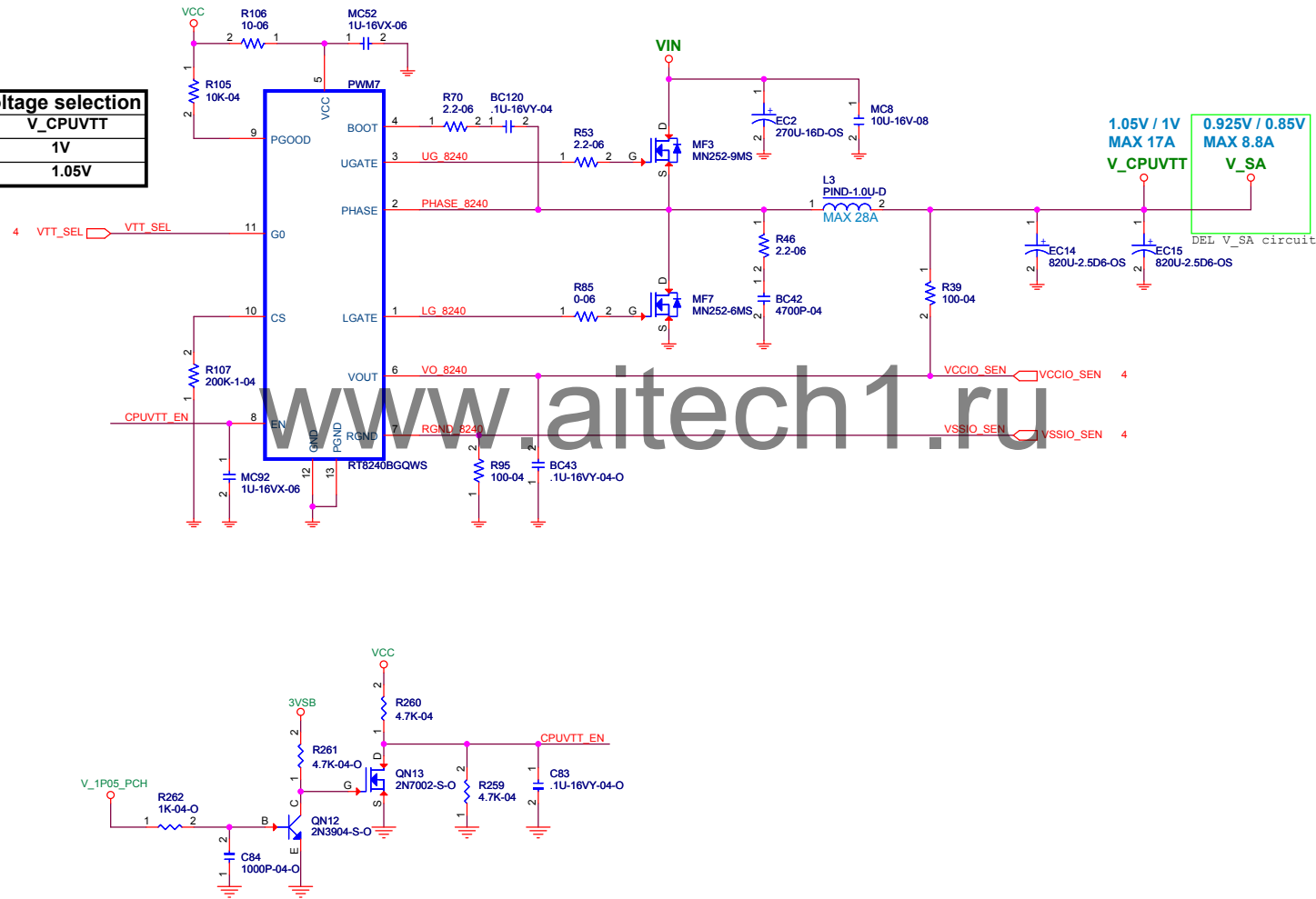
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Size	Document Number	H61H2-M17	
Custom		Rev 1.0	
Date:	Wednesday, May 02, 2012	Sheet	10 of 29

External Connection

VCC	○	○	VCC
3VSB	○	○	3VSB
VIN	○	○	VIN
V_1P05_PCH	○	○	V_1P05_PCH
V_CPUVTT	○	○	V_CPUVTT

VCCIO voltage selection

VTT_SEL	V_CPUVTT
low	1V
high	1.05V



Elitegroup Computer Systems

Title

DC/DC V_CPUVTT/V_SA RT8240B

Size

Document Number

H61H2-M17

Rev

1.0

Date:

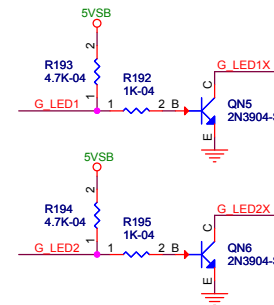
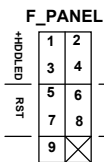
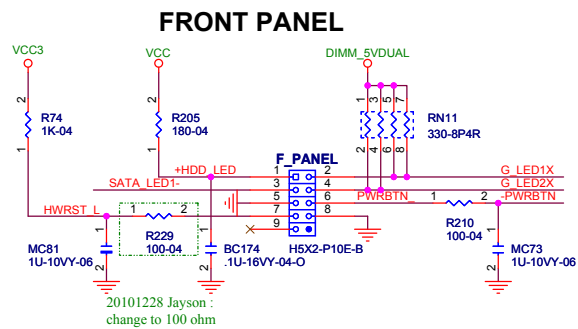
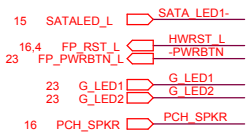
Wednesday, May 02, 2012

Sheet

11

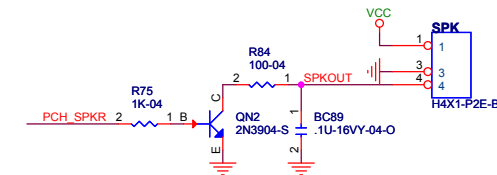
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External Connection

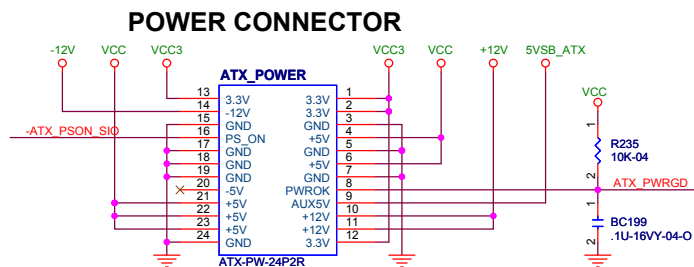
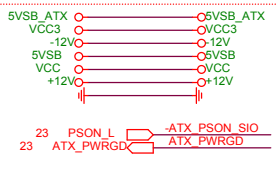


	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	G	GB	YB	OFF	OFF

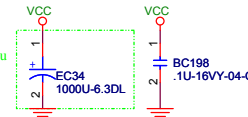
B:Blinking



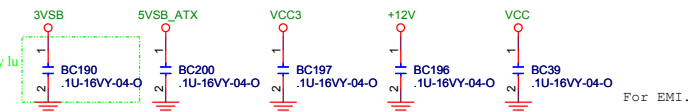
External Connection



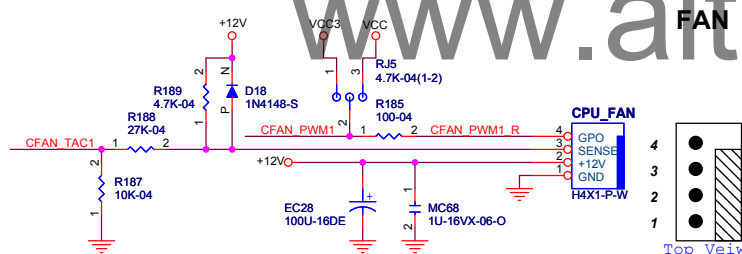
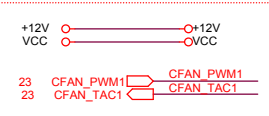
20101029
Add By Andy lu



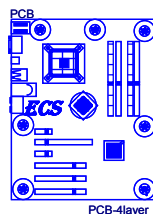
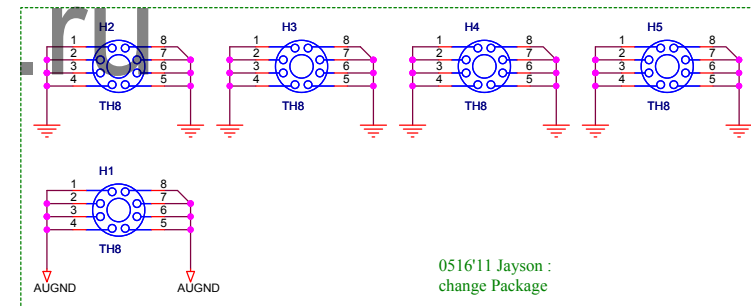
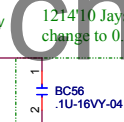
20100929
Change By Andy lu



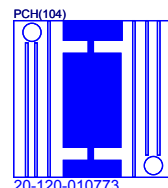
External Connection



121410 Jayson :
change to 0.1U-04

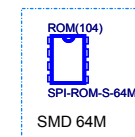
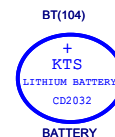


PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM



5 series PN:20-120-010851

0214'11 Jayson :
PCH Heat Sink change to smaller.



20120417 H61H2-M17
change for WIN8.

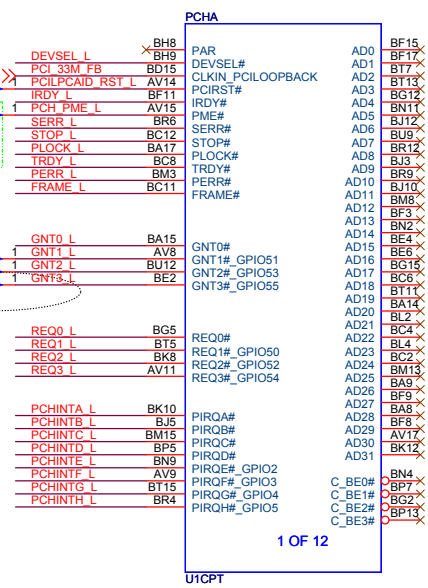


Elitegroup Computer Systems		
Title: Front Panel,FAN,PowerConn,GND,104		
Size: Custom	Document Number: H61H2-M17	Rev: 1.0
Date: Wednesday, May 02, 2012	Sheet: 13	of 29

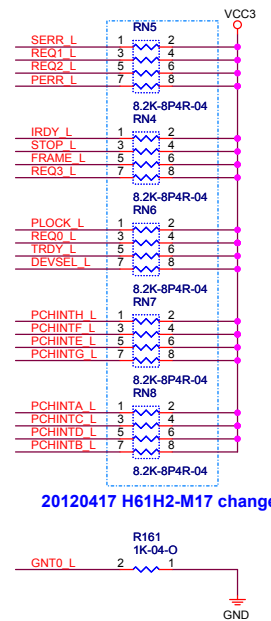
20100910
Add By Andy lu
For Test Point

TP9
TP11
TP10
07/21

20100910
Del By Andy lu
For PCI Slots



01-201-082013



20120417 H61H2-M17 change.

GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ESI Strap (Server Only),
DON'T Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode,
When Sampled Low.

GNT[0..3]# / GPIO19
have been internal pull high to VCC3

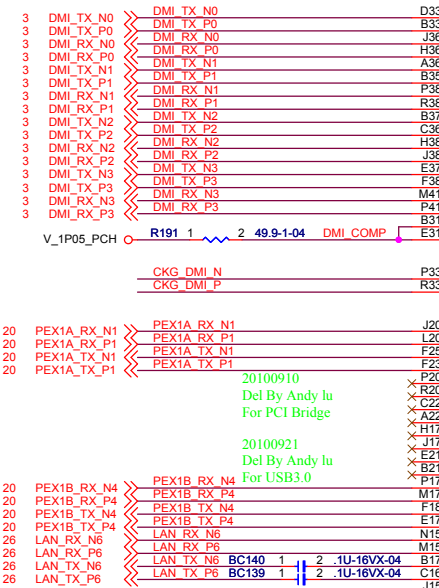
Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

★

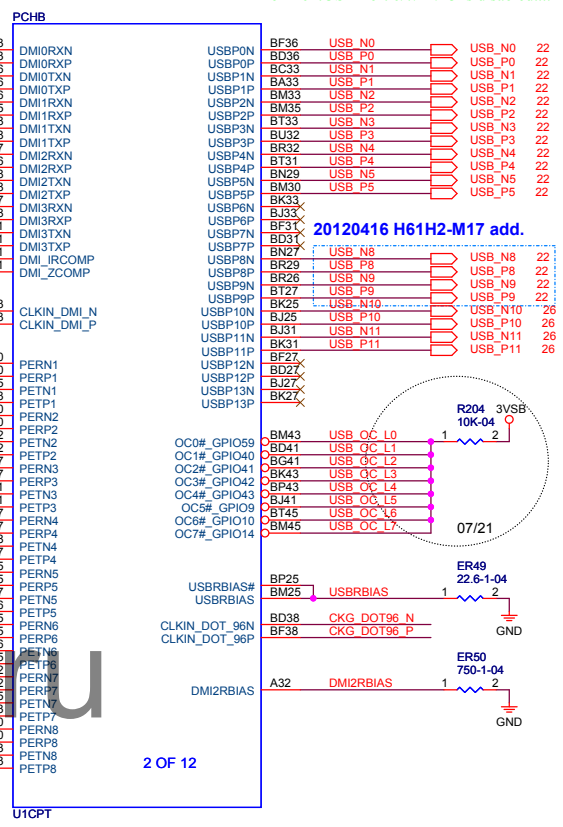
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For H61:PCIE 7/8 is disable....From intel Jasmine

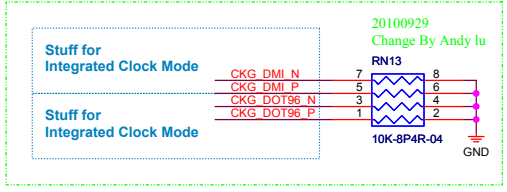


20100910
Del By Andy lu
For PCI Bridge

20100921
Del By Andy lu
For USB3.0



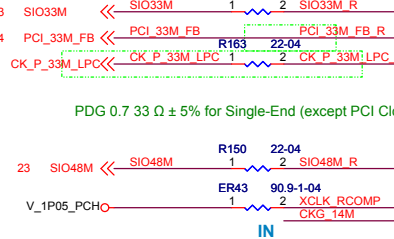
2 OF 12



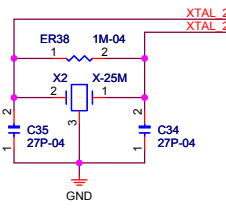
F_USB2
F_USB1
USBx4
USBLAN

For H61:USB Port 6/7/12/13 is disabled....From 440377 file

20100923
Add By Andy lu
For LPC Debug



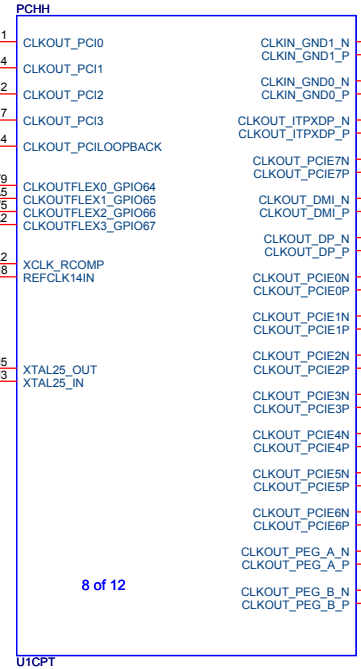
Layout Note:
PCI Clock Max 1500MILS



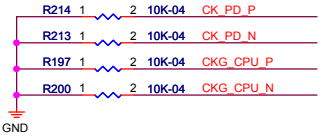
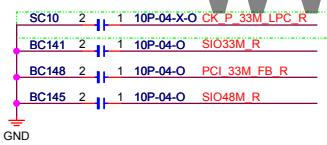
SATA



1207*10 :
By Jayson added



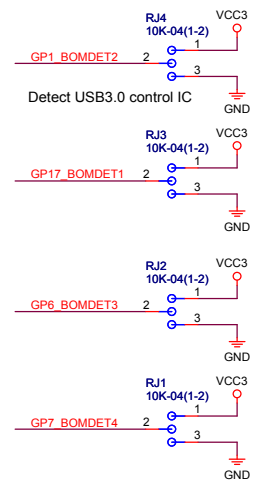
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Stuff for Integrated Clock Mode

Clock Mode	CLK GEN. IDT CV184 Circuit.	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X

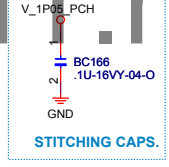
20100923
Add By Andy lu
For LPC Debug



CPU
Jack 08/10

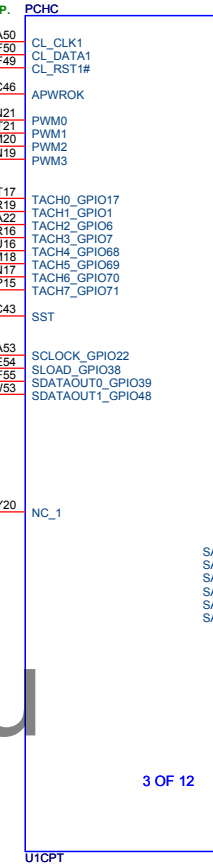
PCIEx1_B
PCIEx1_A

PCIEx16



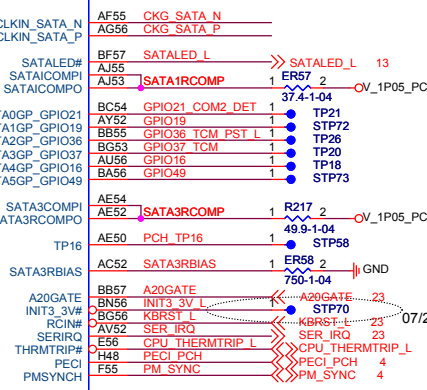
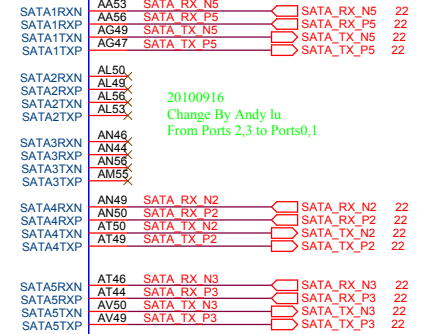
STITCHING CAPS.

MOBILE ONLY,
NOT FOR DESKTOP.

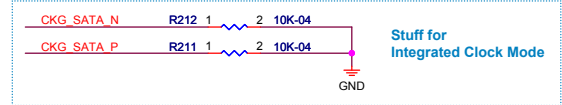
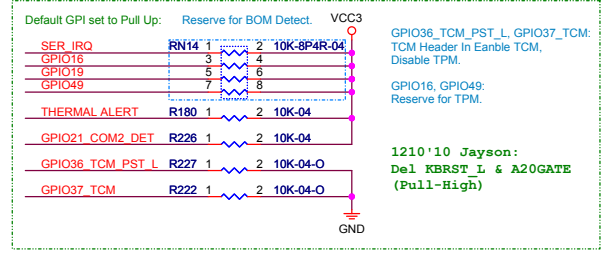


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For H61:SATA port2/3 is disable....From 440377 file
ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.



20120417 H61H2-M17 change.



23 LPC_AD[0..3] LAD[0..3]

1207'10 :
By Jayson added

STP48 1 LPC_DRQ1_L BA20
23 LPC_AD1 LPC_AD0 BK15
23 LPC_AD1 LPC_AD1 BJ17
23 LPC_AD2 LPC_AD2 BJ20
23 LPC_AD3 LPC_AD3 BJ23
23 STP43 LPC_DRQ0_L BK17
23 LPC_FRAME_L LPC_FRAME_L BG17

24 HDA_BITCLK HDA_BITCLK BU22
24 HDA_RST_L HDA_RST_L BC22
24 HDA_SDI0 HDA_SDI0 BD22
BF22
BK22
HDA_SDI0 HDA_SDI0 BJ22
HDA_SDI0 HDA_SDI0 BJ23
HDA_SDO HDA_SDO BP23
HDA_SYNC HDA_SYNC BP23

24 HDA_SDO HDA_SDO BP23
24 HDA_SYNC HDA_SYNC BP23
22 SPI_MOSI SPI_MOSI AU53
22 SPI_MISO SPI_MISO AT55
22 SPI_CS_L0 SPI_CS_L0 AR54
22 SPI_CLK SPI_CLK AR56
22 SPI_CS_L1 SPI_CS_L1 AR56

PCH_RTCX1 BR39
PCH_RTCX2 BR39
RTCX1 RTCX1 BT41
RTCX2 RTCX2 BT41
SRTCST# SRTCST# BN37
INTRUDER# INTRUDER# BM38
PWRGD PWRGD BJ38
RSMRST# RSMRST# BK38
INTVRMEN INTVRMEN BN41
DPWROK DPWROK BT37
DSWODVREN DSWODVREN BR42

20,26,7,8 SMBCLK SMBCLK BN49
20,26,7,8 SMBDATA SMBDATA BR49
SMLK0ALERT# SMLK0ALERT# BU49
SMLK0 LAN_CLK SMLK0 LAN_CLK BT51
SMLK0 LAN_DATA SMLK0 LAN_DATA BM50
SMLK1ALERT# SMLK1ALERT# BR46
SMLK1 SIO_CLK SMLK1 SIO_CLK BJ46
23 SMLK1 SIO_DATA SMLK1 SIO_DATA BK46

23 SMLK1 SIO_CLK SMLK1 SIO_CLK BJ46
23 SMLK1 SIO_DATA SMLK1 SIO_DATA BK46

DSWODVREN R203 1 2 390K-04
INTRUDER_L R201 1 2 1M-04

SMLK0 LAN_DATA RN9 2 2 2.2K-8P4R-04
SMLK0 LAN_CLK 4 3
SMLK1 SIO_CLK 6 5
SMLK1 SIO_DATA 8 7
PCH GP30 RN12 2 1 8.2K-8P4R-04
PCH GP27 4 3
PCH GP31 6 5
PCH GP45 8 7
RI_L RN10 2 1 2.2K-8P4R-04
SMBCLK 4 3
SMBDATA 6 5
LPCPD_L 8 7
SMBALERT_L R218 1 2 10K-04
SMLK0ALERT_L R209 1 2 2.2K-04
SMLK1ALERT_L R208 1 2 10K-04
LPC_PME_L R186 1 2 10K-04
PCIE_WAKE_L R223 1 2 1K-04
RSMRST_L R198 2 1 680-04
BC1701 2 1U-16VY-04-0

DRAM_PWROK ER48 1 2 200-1-04
SPL_CS_L1 R228 1 2 10K-04
PCH_GP20_PU R224 1 2 10K-04
R225 1 2 10K-04-0
PCH_GP45 R207 1 2 10K-04-0

DRAM_PWROK ER48 1 2 200-1-04
SPL_CS_L1 R228 1 2 10K-04
PCH_GP20_PU R224 1 2 10K-04
R225 1 2 10K-04-0
PCH_GP45 R207 1 2 10K-04-0

PCHD

BMBUSY#_GPIO0 CLKRUN#_GPIO32
HDA_DOCK_EN#_GPIO33
STP_PC#_GPIO34
GPIO35

GPIO8
LAN_PHY_PWR_CTRL#_GPIO12
HDA_DOCK_RST#_GPIO13
GPIO15
GPIO24_MEM_LED
GPIO28
SPL_LAN#_GPIO29
PCIECLKRQ2#_GPIO20
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
GPIO57
SYS_PWROK
RI#
PLTRST#
WAKE#
SLP_A#
SLP_S3#
SLP_S4#

GPIO8
LAN_PHY_PWR_CTRL#_GPIO12
HDA_DOCK_RST#_GPIO13
GPIO15
GPIO24_MEM_LED
GPIO28
SPL_LAN#_GPIO29
PCIECLKRQ2#_GPIO20
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
GPIO57
SYS_PWROK
RI#
PLTRST#
WAKE#
SLP_A#
SLP_S3#
SLP_S4#

SUS_STAT#_GPIO61
SUSCLK#_GPIO62
BATLOW#_GPIO72
PWRROK
RSMRST#
INTVRMEN
DPWROK
DSWODVREN

SMBALERT#_GPIO11
SMBCLK
SMBDATA
SMLK0ALERT#_GPIO60
SMLK0 LAN_CLK
SMLK0 LAN_DATA
SMLK1ALERT#
SMLK1 SIO_CLK
SMLK1 SIO_DATA

SUSWARN#_SUSPWROK/GPIO30
DRAMPWROK

TP12
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS

UTCPY

PCH_RTCX1
PCH_RTCX2
Y1 X-32.768K
BC175 18P-04
BC176 18P-04

VBAT_IO
VBAT_IO_S
CLR_CMOS H3X1-R
D11 BAT54C-S
R104 1K-04
BT SK-CR2032-D

AW55 FP_AUD_DETECT
BC56 CLKRUN_L
BC25 HDA_DOCK_EN_L
BL56 PCH_PU_GP34
BJ57 TP_GPIO35

BP51 IGC_EN_L
BK50 LAN_DISABLE_L
BA25 LPC_PME_L
BM55 TLS_EN
BP53 PCH_SKTIOCC_L
BJ55 ON_DIE_PLL_EN
BH49 SLP_LAN_L
AV43 PCH_GP20_PU
BL54 PCH_GP44
AV44 PCH_GP45
BP55 PCH_GP46
BT53 GP57_BV_DETECT
BJ53 PCH_SYSPWROK
BJ48 RI_L
BK48 PCH_PLTRST_L
BC44 PCIE_WAKE_L
BC41 SLPAMT_L
BM53 SLP3_L
BN52 SLP4_L

STP61
LPC_PME_L 23
GPIO15 12
STP65
TP25
STP62

TP17
TP16
VR_READY 9
VR_READY 9

RL_L 21
PCH_PLTRST_L 23
PCIE_WAKE_L 20,26
STP51
SLP3_L 23,4
SLP4_L 23

TP67
TP67
TP66
TP14

TP53
SLP_SUS_L
SIO_PWRBTN_L 23

BE52 SYS_RST_L
BE56 PCH_SPKR
FP_RST_L 13,4
PCH_SPKR 13

D53 CPU_PWROK
CPU_PWROK 4

BC49 PCH_JTAG_RST_R 1
BA43 PCH_JTAG_TCK_R 1
BC52 PCH_JTAG_TDI 1
BC47 PCH_JTAG_TDO 1
BC50 PCH_JTAG_TMS 1

STP69
STP66
TP28
STP68
STP64

INTRUDER_L
H2X1-B

CLR_CMOS

Width 20 mils
R108 20K-04
MC45 1U-10VY-06
ER37 20K-1-04
R104 1K-04
MC47 1U-10VY-06
BC113 1U-10VY-06

Buffer Through Mode /
Integrated Clock Mode
have been changed to F/W Strap.
Default: Integrated Clock Mode
Doc. Cougar Point Platform Controller Hub
(PCH) Family EDS Update V0.7.1

IGC_EN_L R219 1 2 1K-04
GND

Integrated Clock:

IGC_EN_L (internal PU)	
H	Buffer Through Mode
L	Integrated Clock Mode

In Sugar Bay Q series Platform,
Enable TLS for vPro.

TLS_EN

TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

PCH_SPKR

No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

INTVRMEN R202 1 2 390K-04
VBAT_IO

Integrated 1.05V SUS VRM:

INTVRMEN	
H	Enable
L	Disable

When Deep Sleep not implemented:
1.PCH_GP30, PCH_GP27 need to be Pull Up.
2.VCCDSW3_3 should to be connected to +3VSB.
3.SLP_SUS_L, SUSACK_L left unconnected
4.SUSWARN_L may be used as GPIO30.(Reference to 1.)

RSMRST_L DPWROK

For platform not supporting
deep sleep connect directly
to RSMRST#.

20100929
Short By Andy lu

ME_UNLOCK
1 ME_UN_PU
2 HDA_SDO
H2X1-B

ME Enable/Disable

	ME_UNLOCK
1-2	UNLOCK
Float	LOCK

3VSB
PCH_GP44 R220 1 2 10K-04
R221 1 2 10K-04-0
GND

JTAG CLK FILTER:

PCH_GP44	
H	Enable
L	Bypass

PCH_GP46

DFX TEST MODE Rings Oscillator:

PCH_GP46 (internal PU)	
H	Enable
L	Bypass

ON_DIE_PLL_EN

On-Die PLL VR:

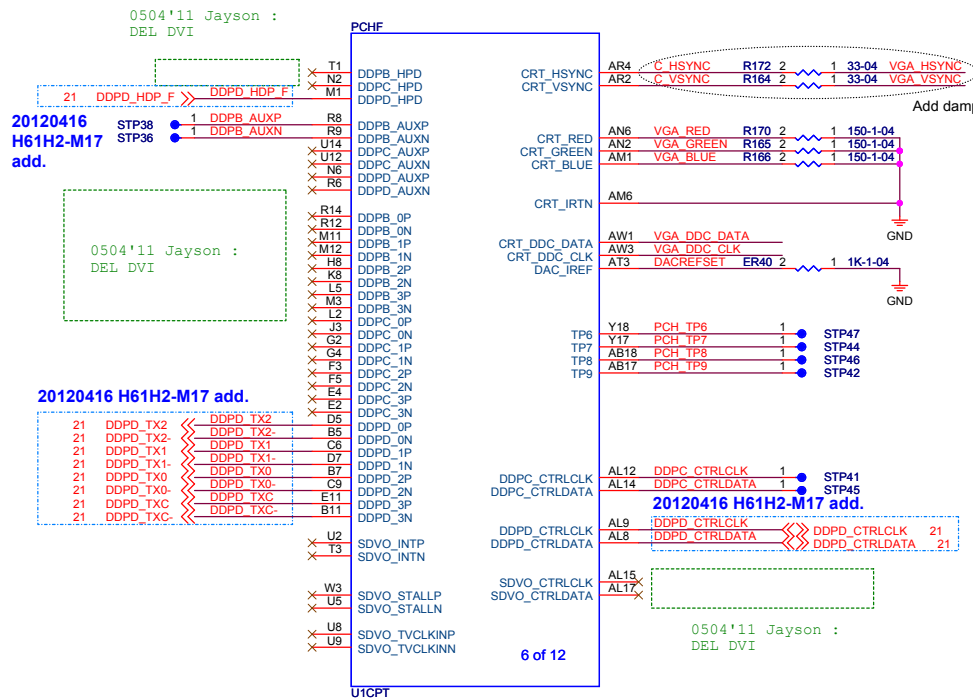
ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

HDA_SYNC

On-Die PLL VR Source:

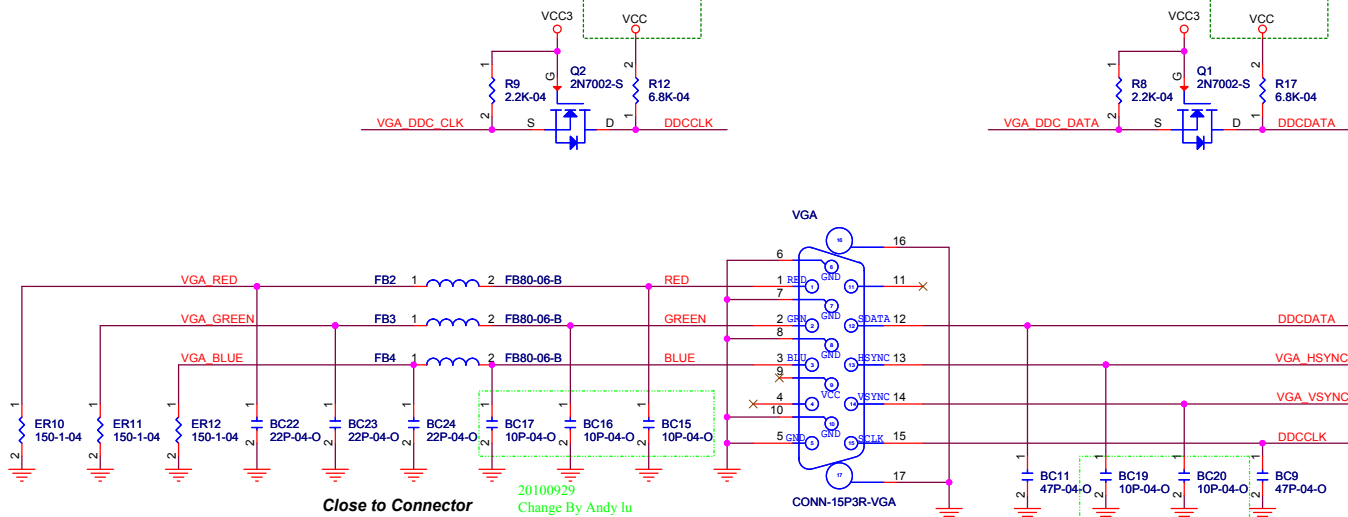
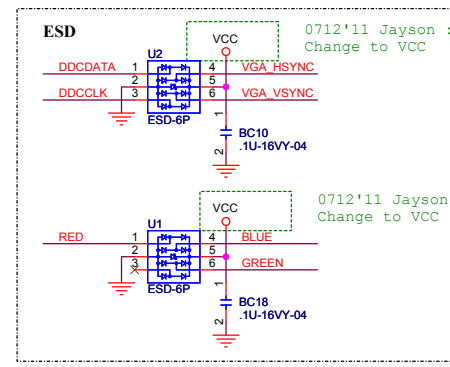
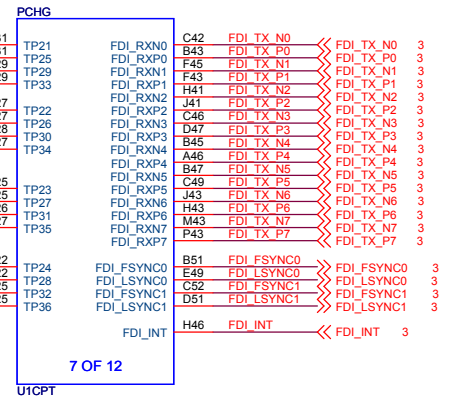
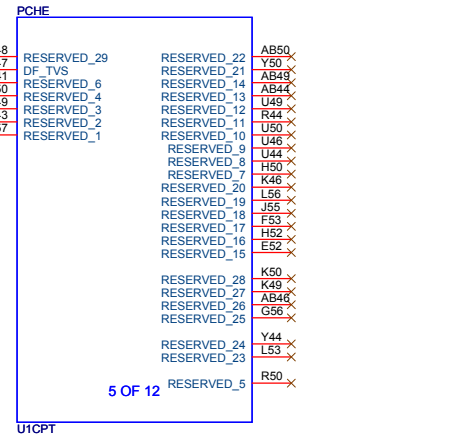
HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

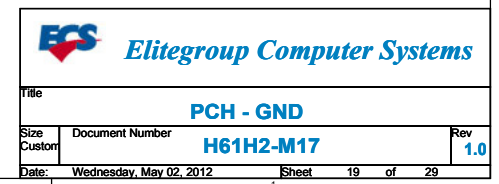
3VSB
R90 1K-04

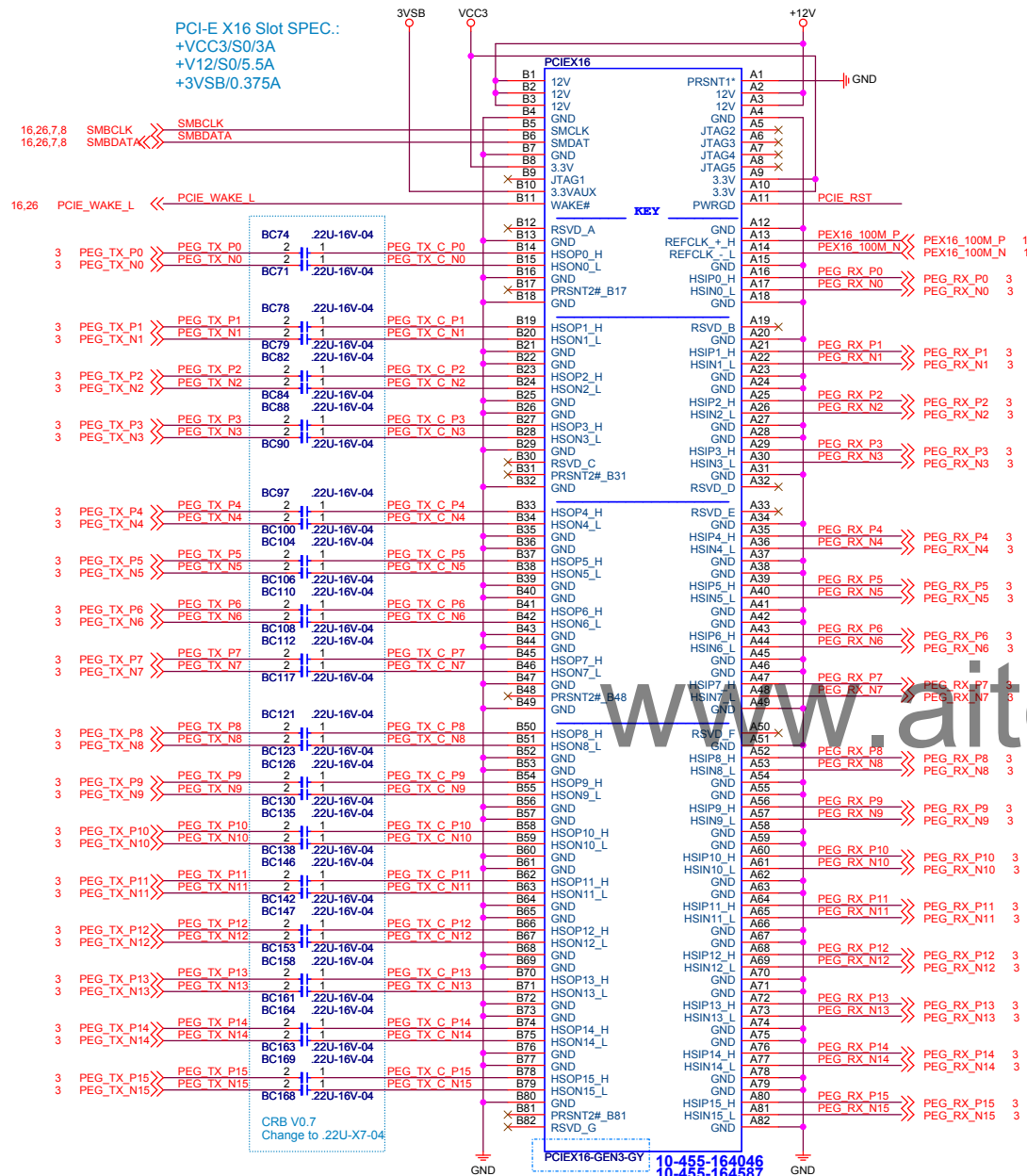


091222 Update!
Terminating unused DC NAND interface:
If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.
Note:
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

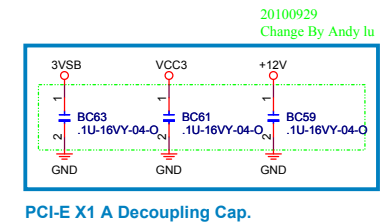
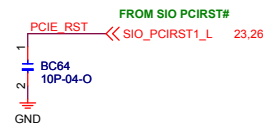
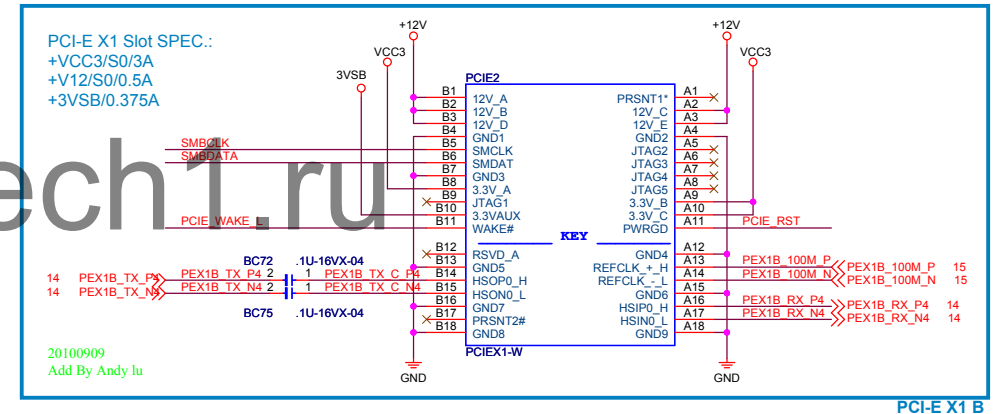
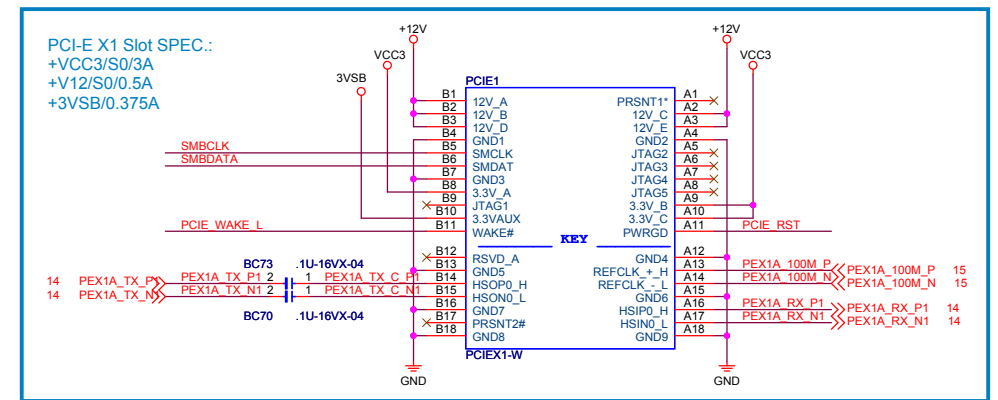
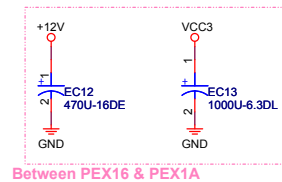
100120 Update!
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip:
Renamed NV_WE#_CK[0:1], NV_RE#_WRB[0:1], NV_RCOMP, NV_RB#, NV_DQ9 / NV_IO[0:15], NV_DQS[0:1], NV_CE#[0:3], and NV_ALE to Reserved(RSVD).
Renamed NV_CLE to DF_TV_S.



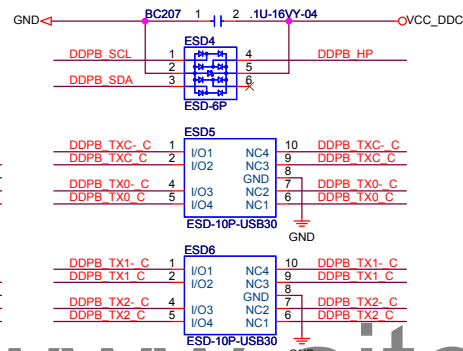
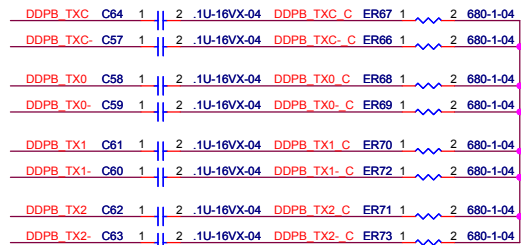
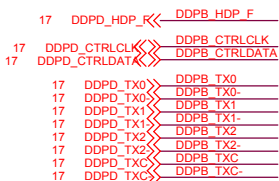




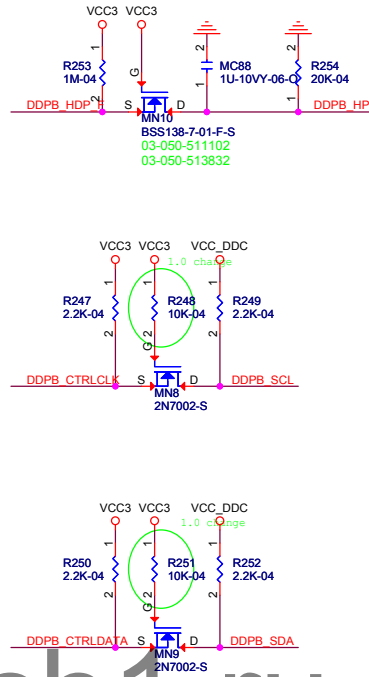
20120417 H61H2-M17 change.



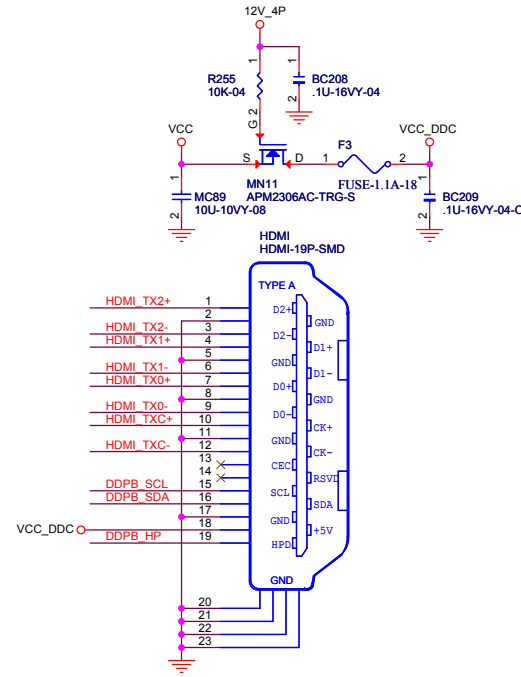
External Connection



HDMI



20120416 H61H2-M17 add HDMI circuit.



DVI

0504'11 Jayson :
DEL DVI

0504'11 Jayson :
DEL DVI

0504'11 Jayson :
DEL Fuse & Diode

0504'11 Jayson :
DEL DVI

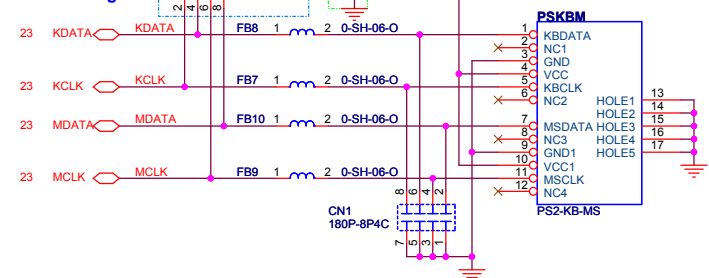
0504'11 Jayson :
DEL DVI

0504'11 Jayson :
DEL DVI Connector

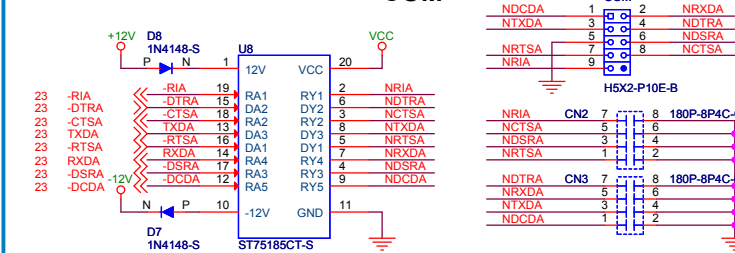
1202'10 Jayson :
Del HDMI

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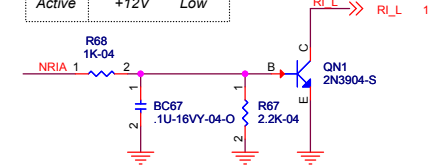
20120417 H61H2-M17 change.



COM

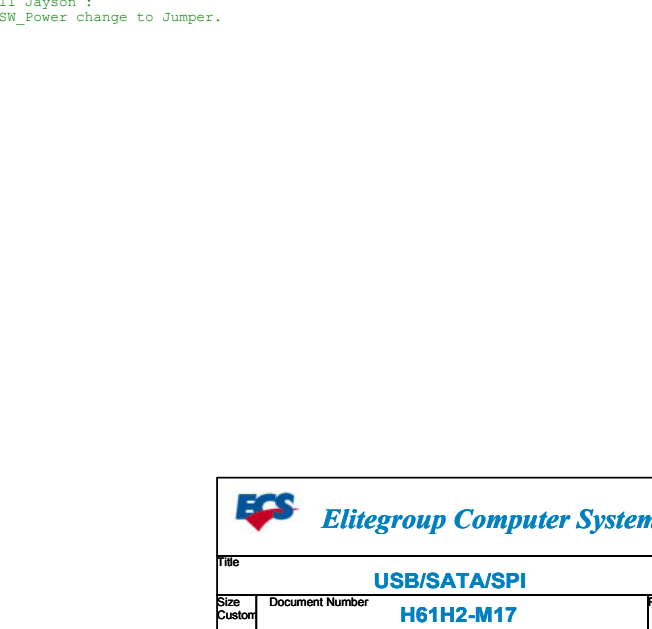
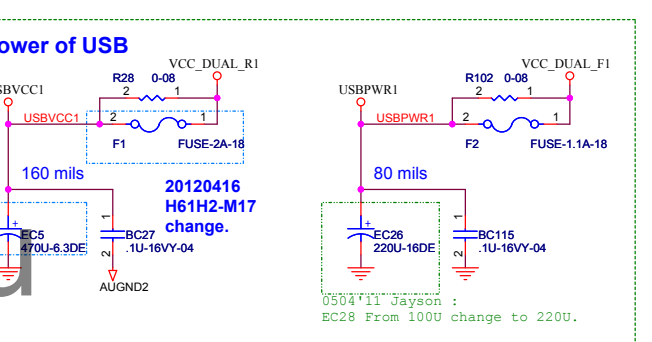
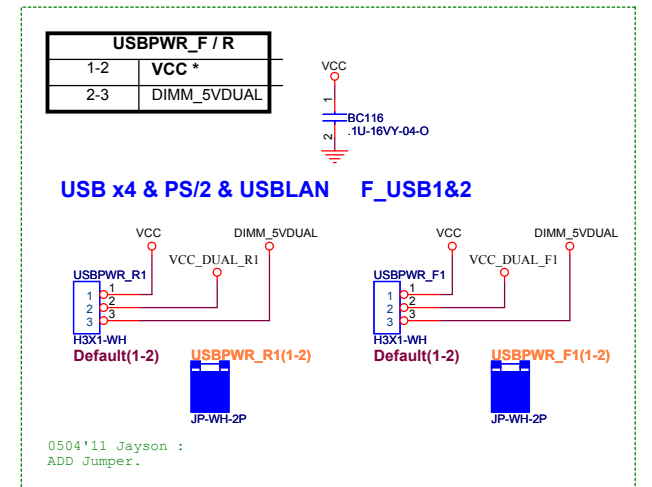
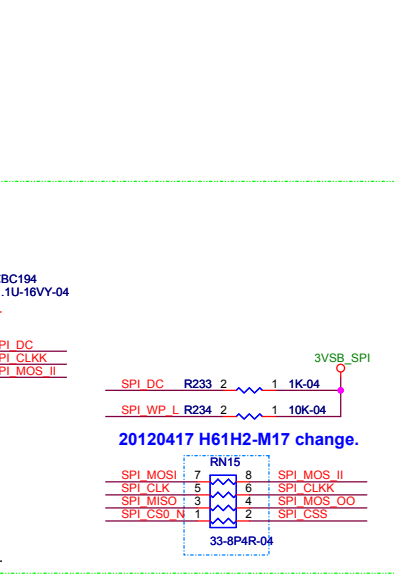
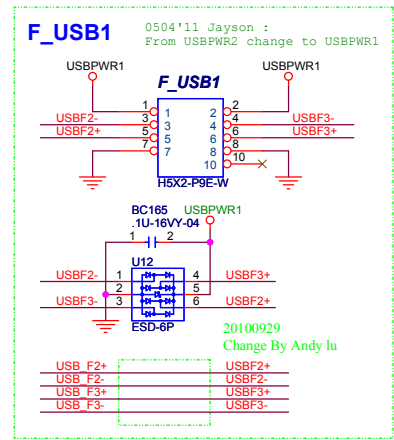
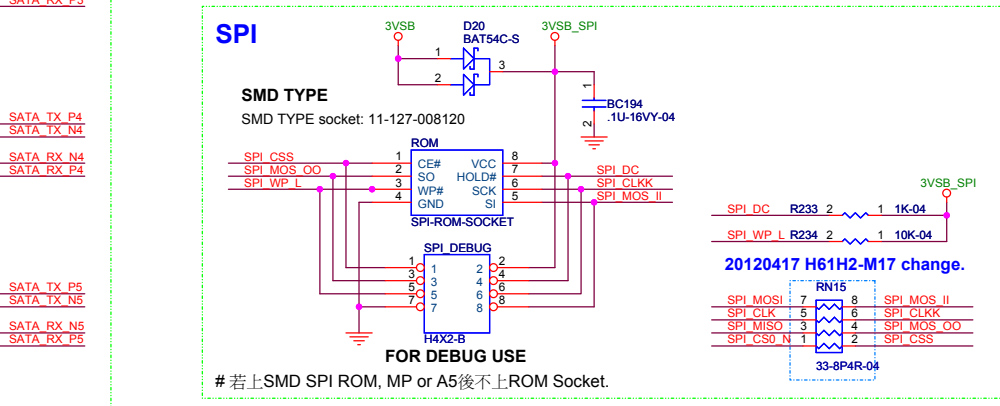
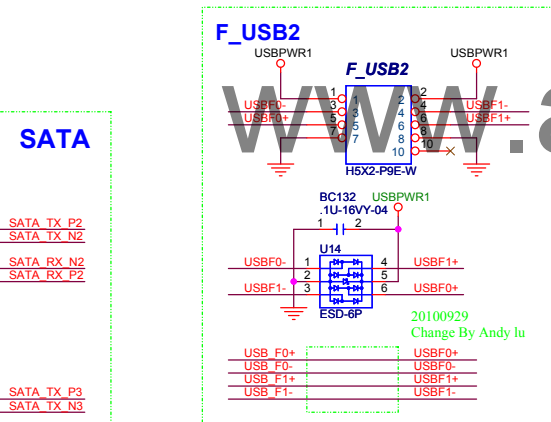
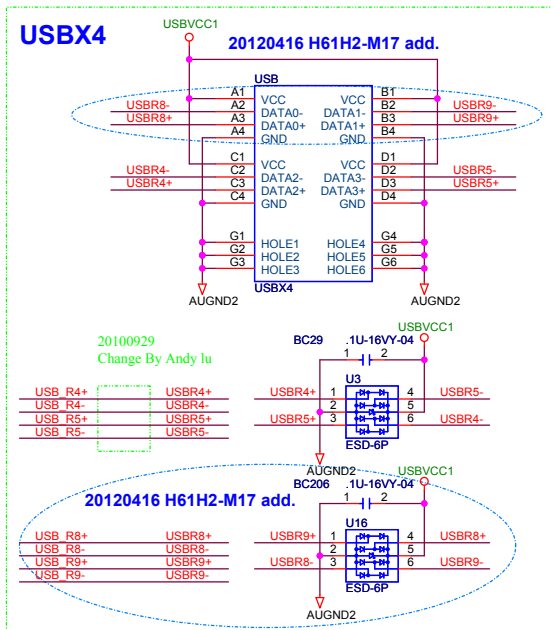
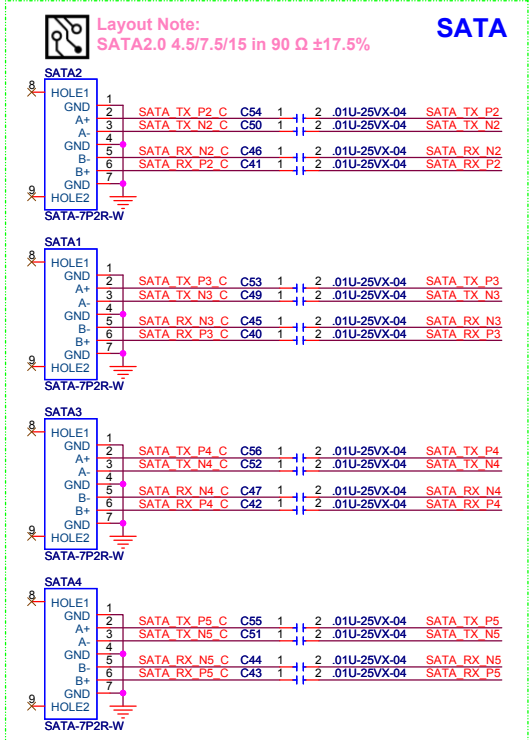
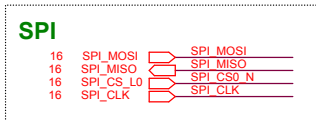
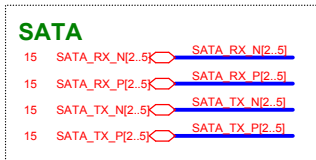
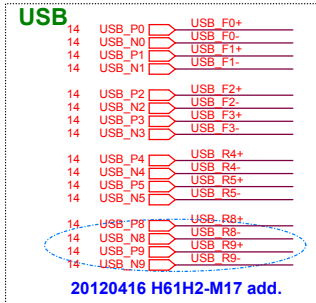


	NRIA	R#
Normal	-12V	High
Active	+12V	Low

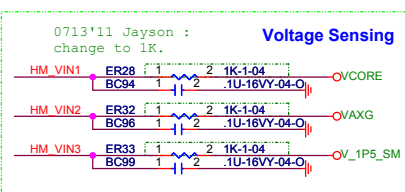
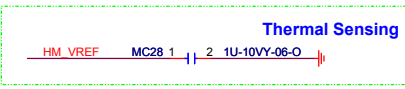
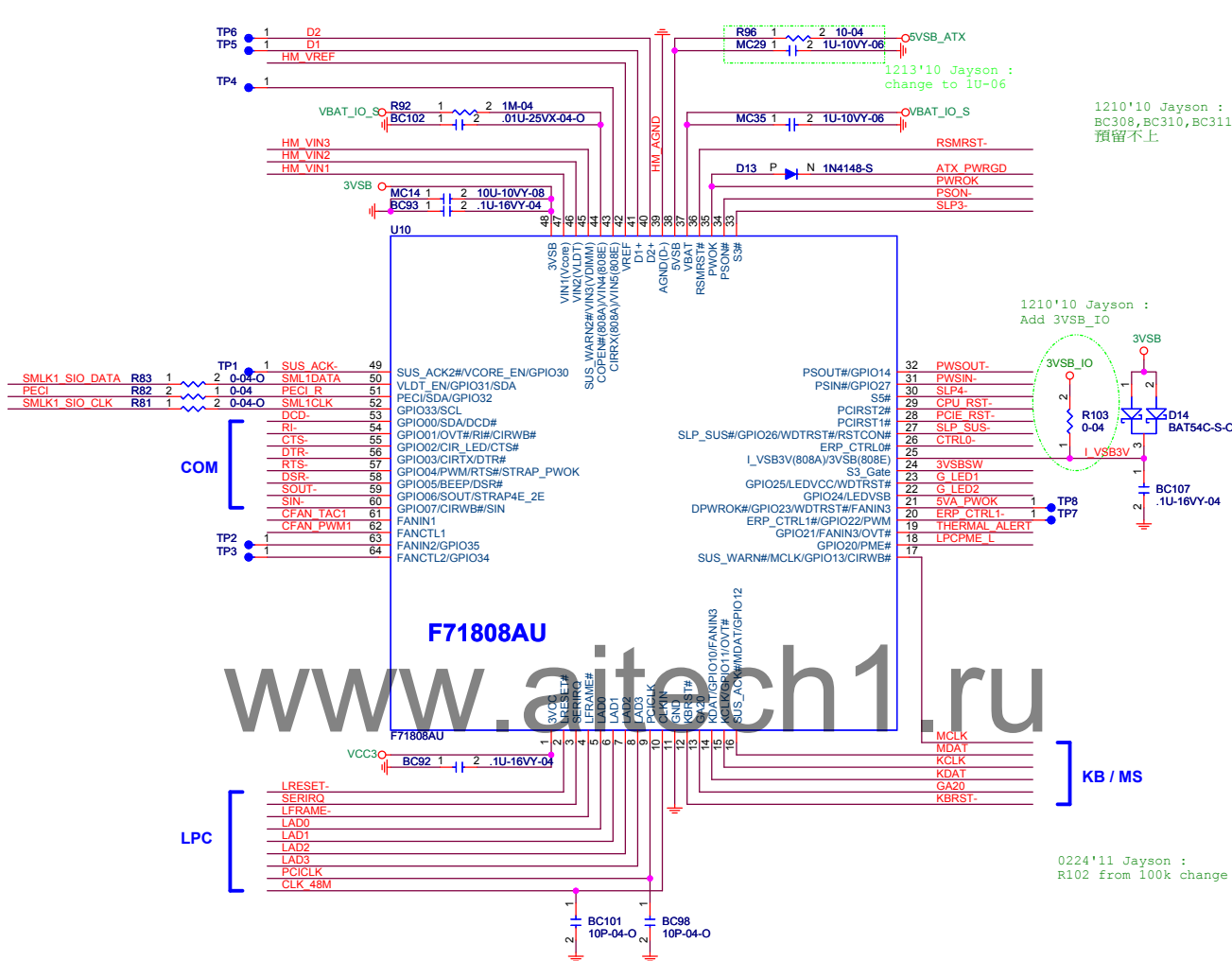
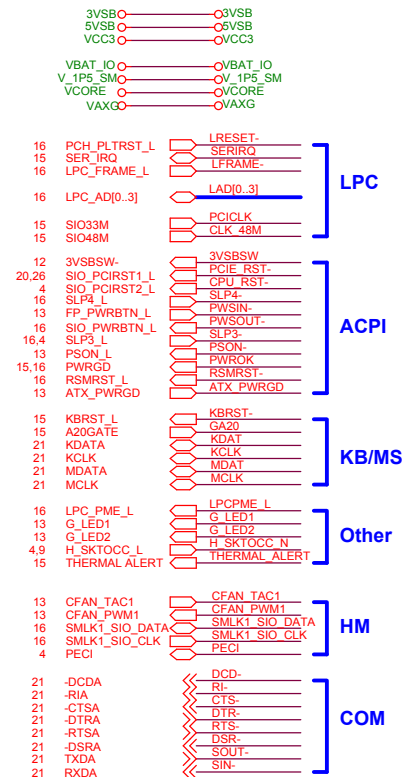


Elitegroup Computer Systems

Title	HDMI / COM / PS2
Size	Document Number
Custom	H61H2-M17
Date	Wednesday, May 02, 2012
Sheet	21 of 29
Rev	1.0



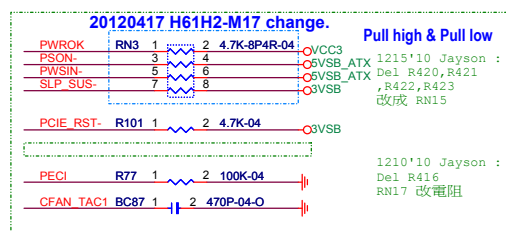
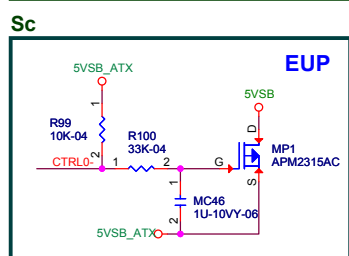
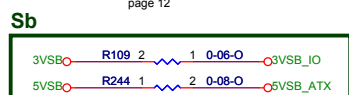
External Connection



EUP

	W/O EUP	W EUP
Sb	V	X
Sc	X	V
Sd	X	V

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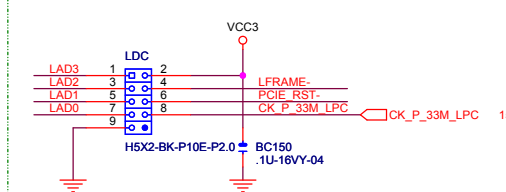
Power On Strapping



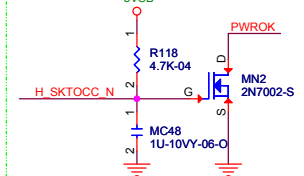
PIN NO.	Symbol	Value	Description
PIN 59	STRAP4E_2E	1	Configuration Register I/O port is 4E/4F.(Default)
		0	Configuration Register I/O port is 2E/2F.
PIN 57	STRAP_PWOK	1	PWOK(pin 35) for AMD(Default)
		0	PWOK(pin 35) for Intel

1231'10 Jayson :
LDC take the place of TPM.

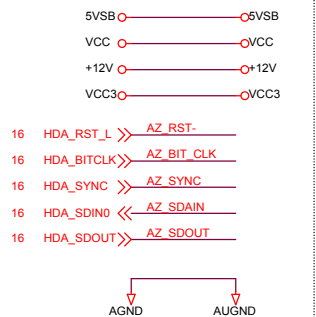
LPC DEBUG HEADER



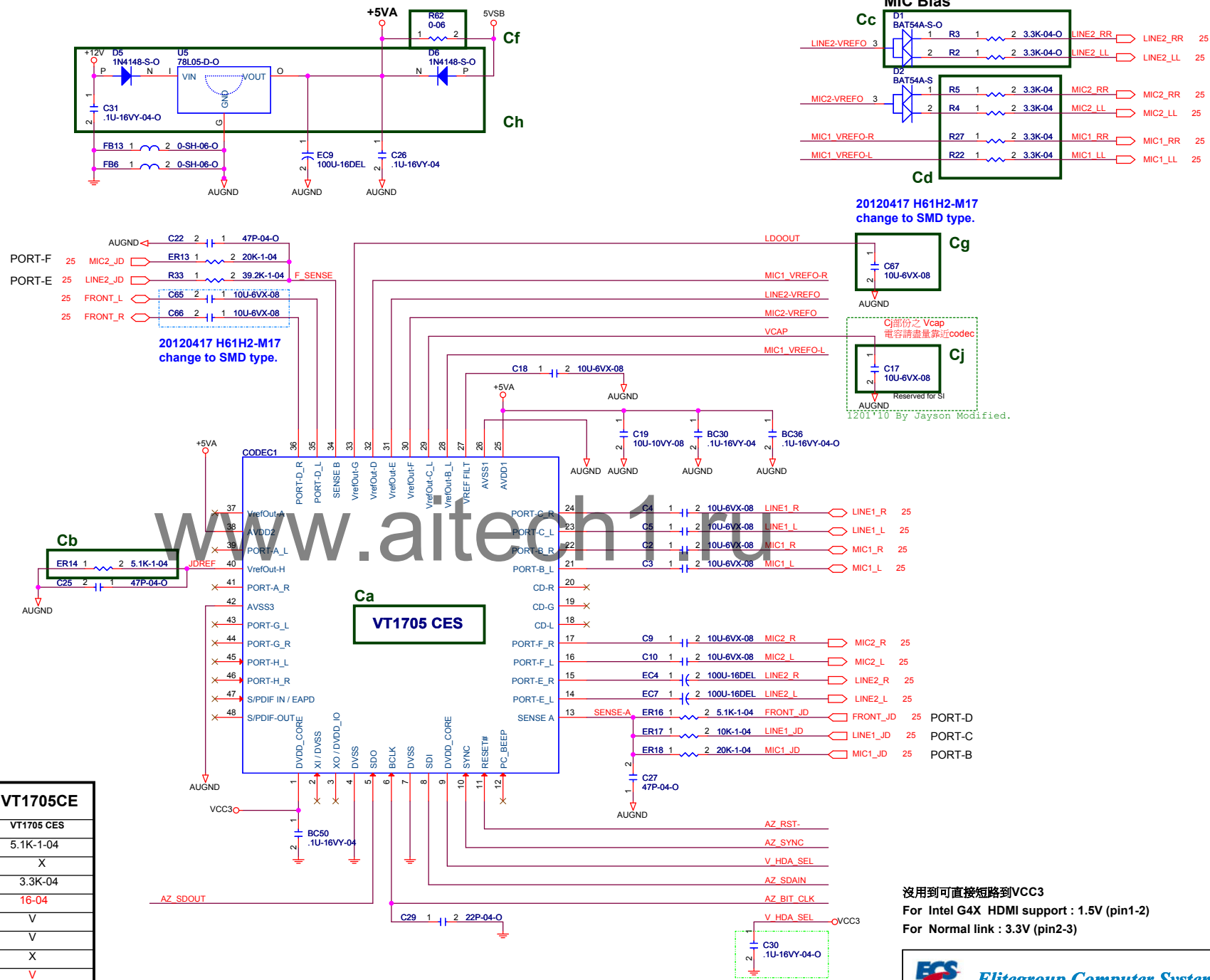
Electric Test



External Connection



* VCC1.5 can remove for non-Intel G4X platform



BOM Difference

Location	ALC662	VT1705CD	VT1705CE
Ca	ALC662-VC-GRS	VT1705CD	VT1705 CES
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	16-04	16-04
Cf	X	X	V
Cg	X	V	V
Ch	V	V	X
Cj	X	X	V
Ck	75-04	33-04	33-04

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

沒用到可直接短路到VCC3

For Intel G4X HDMI support : 1.5V (pin1-2)

For Normal link : 3.3V (pin2-3)

AUDIO VT1705/ALC662 (CHIP)		
Size	Document Number	Rev
Custom	H61H2-M17	1.0
Date:	Wednesday, May 02, 2012	Sheet 24 of 29

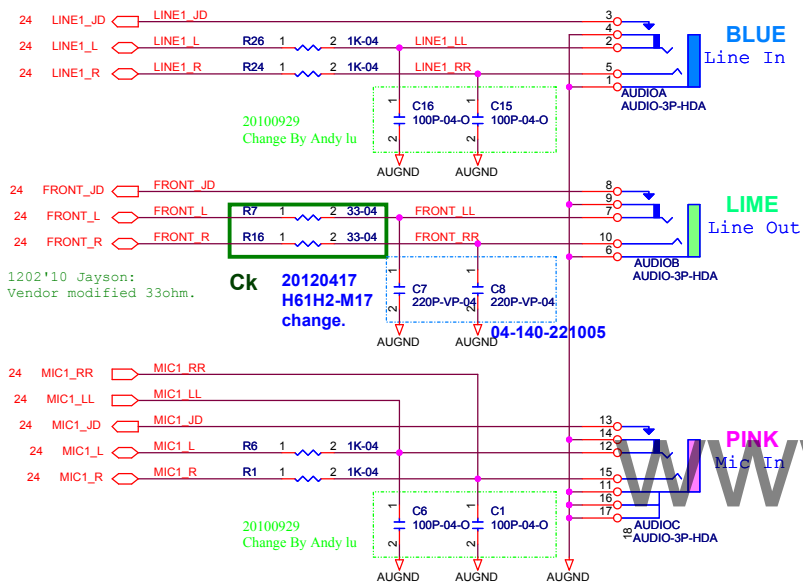
20100929
Change By Andy lu

External Connection

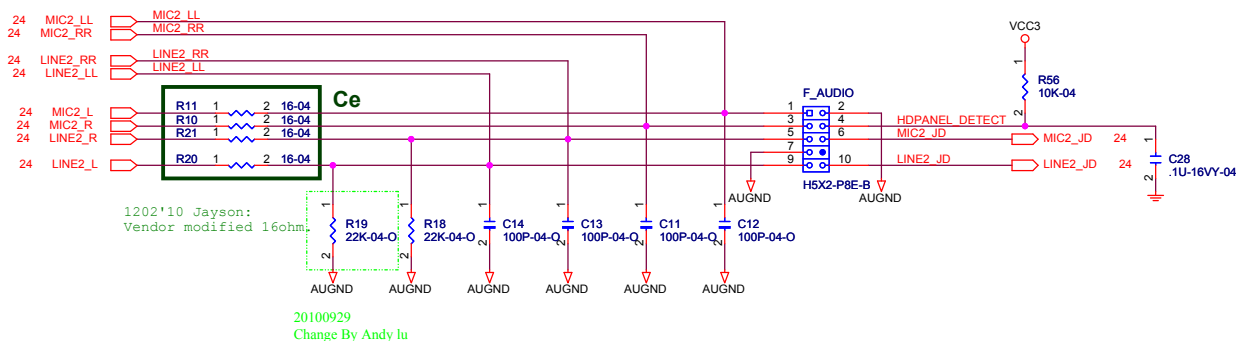
16 FP_AUD_DETECT << HDPANEL_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

REAR-AUDIO Non re-tasking for rear panel

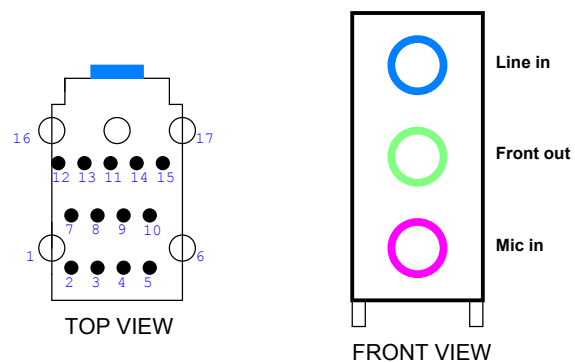


FRONT-AUDIO

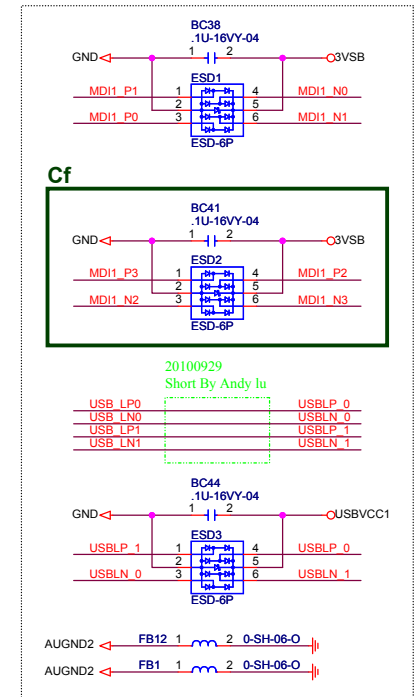
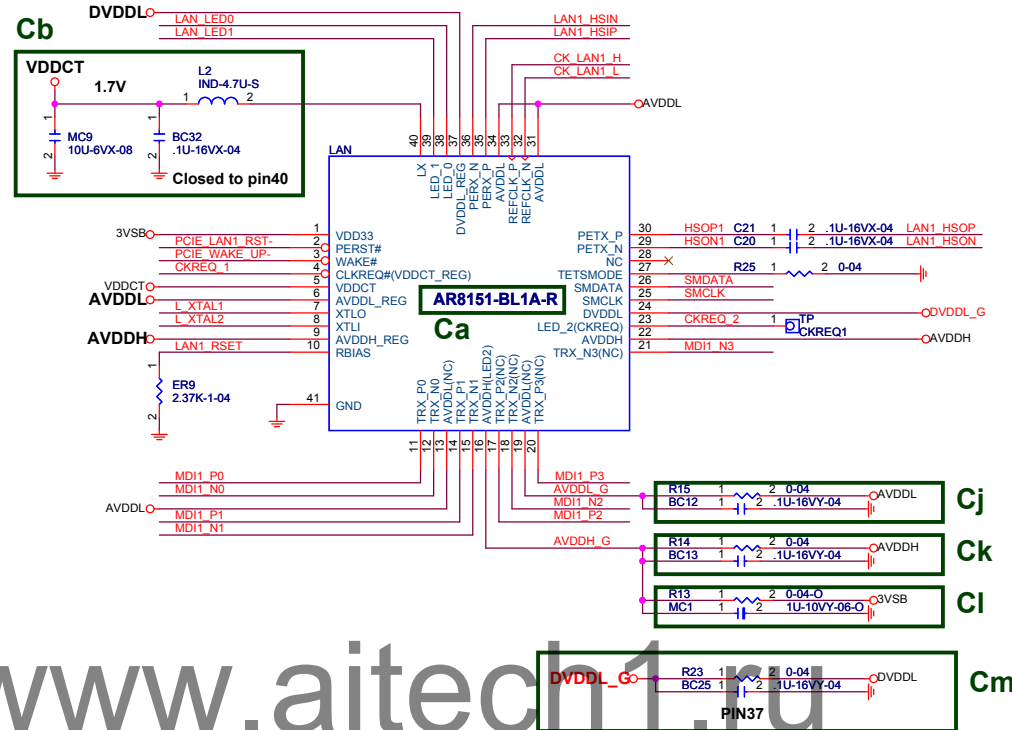
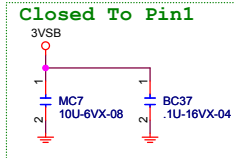
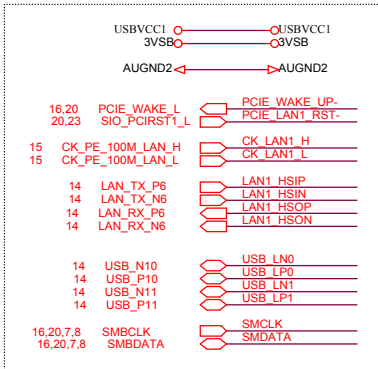


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1203'10 Jayson: Del SPDIF-OUT

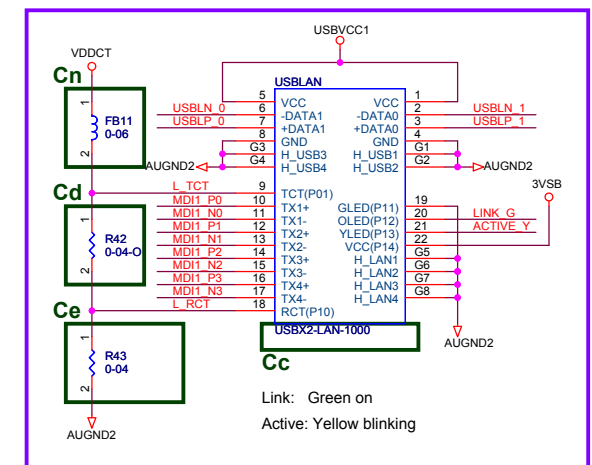
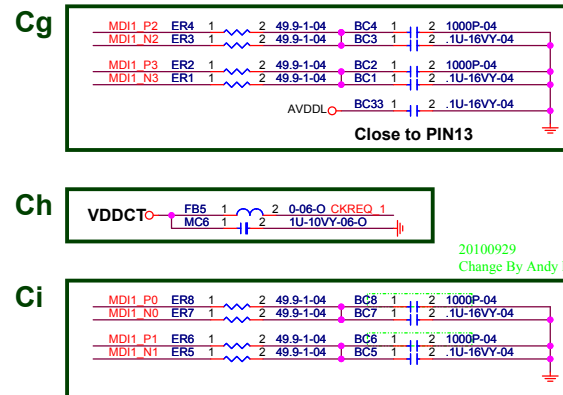
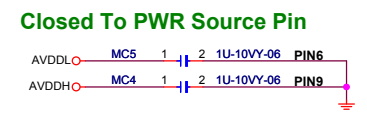
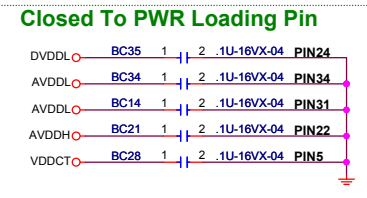
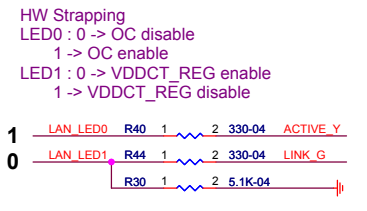


External Connection



BOM Difference

	AR8151-B 1000M	AR8152-B 10/100M	AR8161-B 1000M
Ca	AR8151-BL1A-R	AR8152-BL1A-R	AR8161-B
Cb	V	X	X
Cc	USBX2-LAN-1000	USBX2-LAN-100	USBX2-LAN-1000
Cd	X	V	X
Ce	0-04	.01U-25VX-04	0-04
Cf	V	X	V
Cg	V	X	X
Ch	X	V	X
Ci	V	V	X
Cj	V	X	V
Ck	V	X	X
Cl	X	X	V
Cm	V	V	X
Cn	V	V	X



ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P
12V
+/-5%

Switching RT8859M 4 phases

Switching RT8240B 1 phase

Switching APW 7120

DDR3 DIMM (2) 1333MHz	
VDDQ	15A_S0 1.0A_S3
V_SM_VTT	1.0A_S0

LDO APL5336

Linear OP358

Intel Sandy Bridge CPU		
VCCP	VID 0.25~1.52V	85A(95W)
VAXG	VID 0.25~1.52V	25A
VTT	1.05V(1V)	8.5A
VCC_SA	0.925V(0.85V)	8.8A
VCCPLL	1.8V	1A
VDDQ	1.5V	4.5A

Intel Cougar Point (TDP 5.5W)		
V_PROC_IO	1.05V	1mA
VccDMI	1.05V	0.057A
VccCORE	1.05V	1.6A
VccIO	1.05V	4.07A
VccADPLLA	1.05V	0.1A
VccADPLLB	1.05V	0.1A
VccCLKDMI	1.05V	0.02A
VccSSC	1.05V	0.105A
VccDIFFCLKN	1.05V	0.055A
VccASW(ME)	1.05V	1.61A
VccDFTerm	1.8V	0.2A
VccVRM	1.8V	0.159A
Vcc3_3	3.3V	0.409A
VccADAC	3.3V	0.068A
VccSPI	3.3V	0.02A
VccDSW3_3	3.3V	0.003A
VccSUS3_3	3.3V	0.097A
VccSUSHDA	3.3V	0.01A
VccRTC	3.3V	6uA(G3)
V5REF	5V	1mA
V5REF_SUS	5V	1mA

LAN AR8151 / 52 / 61		
VDD33	3.3V	TBD
internal VDDCT	1.7V	TBD
internal VDDL	1.1V	TBD

SUPER I/O F71808A		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
BAT 3.3V	3.3V	TBD

AUDIO VT1705CE		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

Fans
12V_200mA

SPI
VCC3_30mA

HDMI
VCC_1A fuse

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

Battery
3V

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X16 PCIe Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

Total 1 Slot

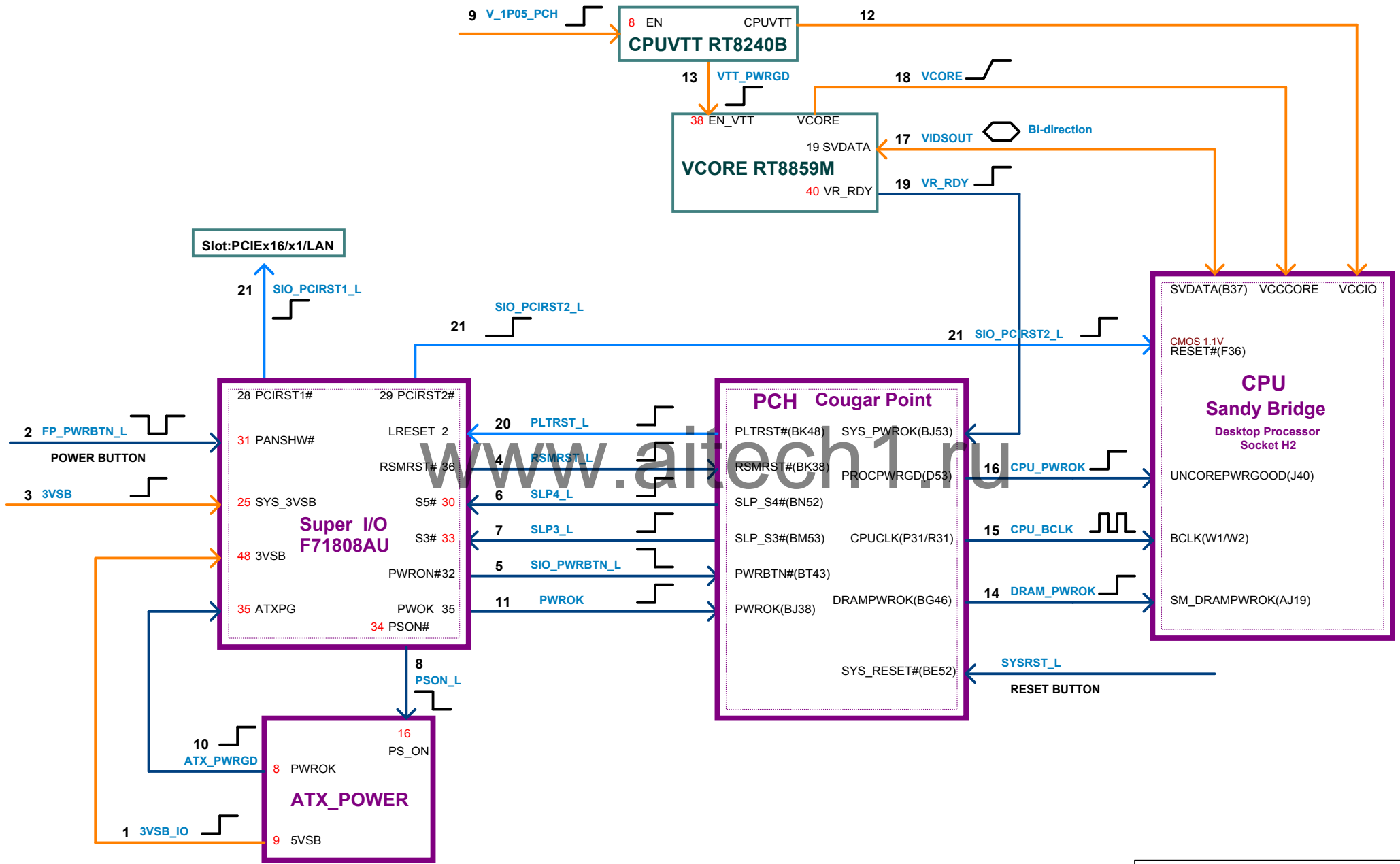
X1 PCIe Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

Total 2 Slots

USBPWR_R1 USBPWR_F1 JUMPER

USB X4 Header
VDD
5VDual
2.0A

USB X6 IO
VDD
5VDual
2.0A



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

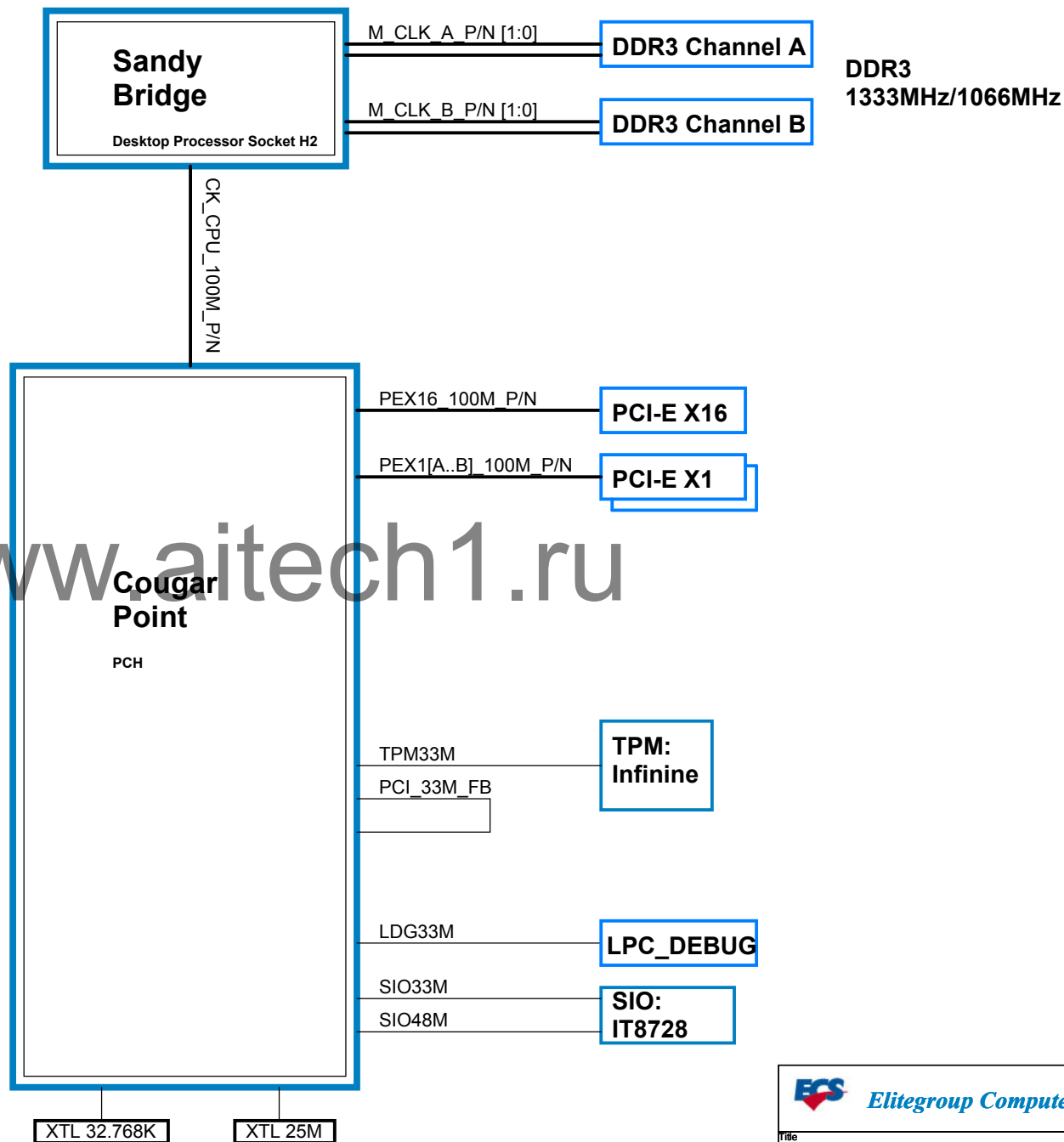
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

1129'10 By Jayson modified



1129'10 By Jayson Del CK505